Titan2 Series products
10G MAC+PCS IP
User Guide

（UG052008,V1.1）

（2023-04-30）_

Document version revision history

date	Document version	Revision history	Applicable IP and corresponding versions
2022-12-30	V1.0	1. initial version.	V1.0
2023-04-30	V1.1	1. Add V1.1 The IP corresponding to the version Version change record; 2. Update applicable device description, see Table 2-1 ; 3. For updated software version requirements, see " Note "; 4. Update the resource utilization typical value table, see Table 2-4 ; 5. Improve IP interface description and update i_tx_axi4s_tuser Port description, add Flow Control Function Related ports , improve PAUSE Flow Control Signals Related port descriptions, adding some status signals and HSSTHP ports, see Table 2-9 ; 6. Standard format.	V1.1

IP Version change history

IP Version	Release Notes	release time
V1.0	1. PG2T 10G MAC+PCS IP initial version.	2022-12- 30
V1.1	1. Optimize IP logic; 2. UG renew.	2023-04- 30

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Figure catalog

Chapter 1 Preface

This chapter describes the scope of application, manual structure, and related writing conventions of this manual to help users quickly find the information they need.

About this manual

10G launched by Unisoc MAC+PCS IP Product User Guide for Titan2 series of FPGA products. The contents of this manual mainly include IP usage guidelines and related appendices. Through this manual, users can quickly understand the related features and usage of 10G MAC+PCS IP .

Manual writing standards

Table 1-1 Writing specifications

Word	Usage principles
Notice	If the user neglects to pay attention to the content, it may cause certain adverse consequences due to misoperation or Unable to operate successfully.
illustrate	Instructions and tips provided to users.
recommend	Recommended settings and usage instructions for users.

Chapter 2 IP usage guide

This chapter talks about 10G MAC+PCS IP Related usage guides, including IP Introduction, IP Block diagram, IP Generation process , Example Design , IP interface description, IP register description, typical applications, instructions and precautions, and IP debugging methods. For more detailed information about the design process, please refer to the following PDS help document.

- *Pango_Design_Suite_Quick_Start_Tutorial* [1]
- *Pango_Design_Suite_User_Guide*[2]
- *IP_Compiler_User_Guide*[3]
- *Simulation_User_Guide*[4]

IP introduction

10G MAC+PCS IP It is based on Titan2 created by Ziguang Tongchuang Series FPGA Implemented for 10GBASE-R Physical Layer Ethernet IP , mainly implements MAC Client Data MAC Packet Encapsulation, decapsulation functions and 10GBASE-R physical layer. Users can use the company's PDS (Pango Design The IPC (IP Compiler) tool in the Suite completes the configuration and generation of IP modules.

Main features

10G MAC+PCS IP is in accordance with IEEE Std 802.3-2018 and IEEE Std 802.1Qbb Standard designed IP ,

The main features are as follows.

- Compliant with IEEE Std 802.3-2018 About 10G Ethernet system standard description;
- Support AXI4-Stream 64bit Data input and output interface;
- Support APB User configuration interface;
- Support MDIO User configuration PHY interface;
- Support 10GBASE-R Physical Layer ;

- SupportDeficit _ Idle Count ;
- Support performance statistics function;
- Support 802.3 and 802.1Qbb FlowControl ; _
- Support VLAN and Jumbo Frames ;
- SupportCustom _ Preamble Mode ;
- Support TX and RX Maximum frame length configuration function.

Applicable devices and packages

table 2-1 10G MAC+PCS IP Applicable devices and packages

Applicable devices	Support packaging type
PG2T390H	ALL
PG2T390HX	ALL

IP block diagram

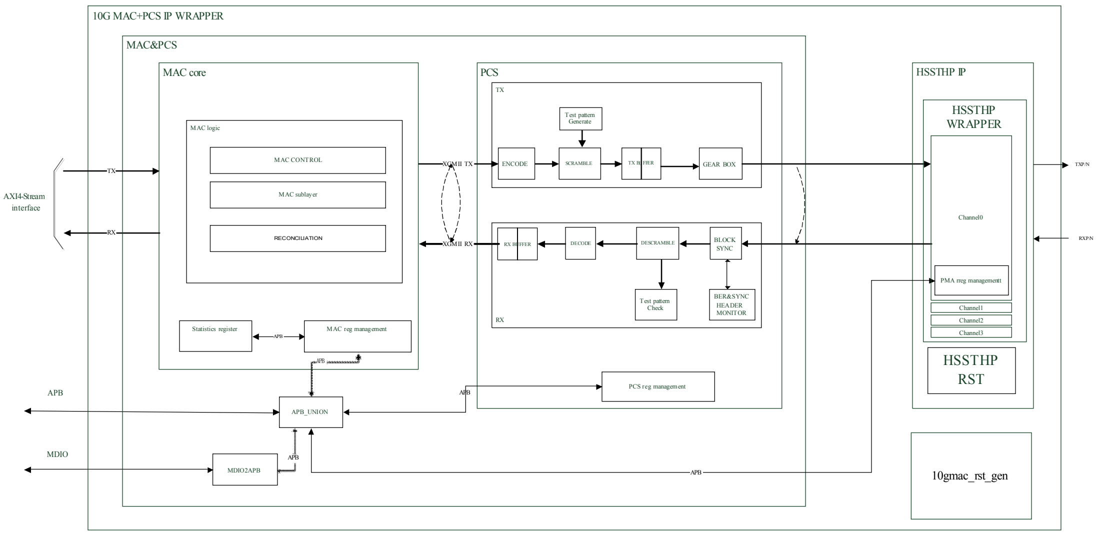


Figure 2-1 10G MAC+PCS IP System Block Diagram

10G MAC+PCS IP by MAC&PCS and HSSTHP _ IP It consists of two parts. The system block diagram is shown in Figure 2-1 .

shown.

MAC & PCS

MAC&PCS Contains MAC Core and PCS Two parts.

1. MAC Core

- In the sending direction, set the MAC client Via AXI4-Stream The transmitted data is encapsulated in compliance with the protocol

  Packet , and then through XGMII Transfer to PCS ;

- In the receive direction the PCS Received Packet byXGMII _ The interface transmits to the MAC , and the MAC Decapsulate it into data and then transmit it to MAC Client through AXI4-Stream .

2. PCS

- XGMII in send direction Tx The transmitted data will be 64B/66B Encode, scramble, and convert to the 64-bit data width required by HSSTHP IP ;
- In the receiving direction, the 64bit The parallel data is 66bit Block _ Lock , descramble, and then perform 64B/66B

  Decoding, via XGMII RX Transfer to MAC Core .

HSSTHP IP

HSSTHP IP by 10G MAC+PCS IP Instantiated on demand, HSSTHP IP for PCS Bypass .

- HSSTHP WRAPPER Contains 4 Channel , each Channel Contains its corresponding PMA , 10G MAC+PCS IP Use Channel 0 As a high-speed serial data transmission channel, for MAC&PCS Provide 64bit of parallel data, and converting MAC&PCS Provided to HSSTHP IP 64bit parallel data serialization .
- HSSTHP RST For the reset sequence, power-on / reset control is completed. This module will be MAC&PCS Provides a logic reset.

IP Generate process

Module instantiation

Via IPC Tools can complete 10G MAC+PCS IP Customized configuration to instantiate the required IP module. For specific usage of IPC tools, please refer to *IP_Compiler_User_Guide* [3] .

10G MAC+PCS IP The main steps of module instantiation are described below.

1. Select IP

Open IPC and click File->Update in the main window OpenUpdate _ IP dialog box, add the corresponding version

IP Model.

Select FPGA After the device type, Catalog The interface can display the mounted IP Model. Select System/Ethernet The corresponding version of 10G in the directory MAC+PCS , IP Select the path as shown in Figure 2-2 shown. Then set the Pathname and Instance Name on the right page . The project instantiation interface is shown in Figure 2-3 . shown.

Notice:

PG2T390H： Software recommendation is 2022.2 and above versions.

PG2T390HX： Software must use 2023.1 and above versions.

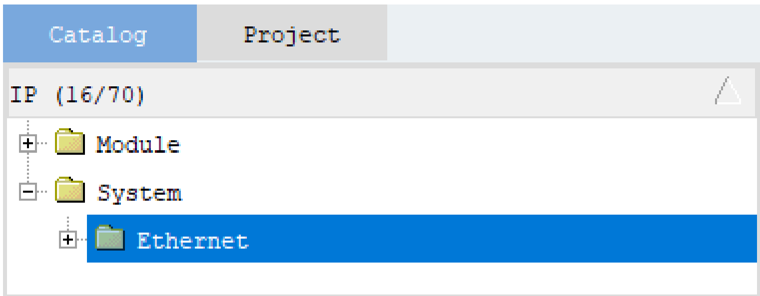


Figure 2-2 10G MAC+PCS IP Select path

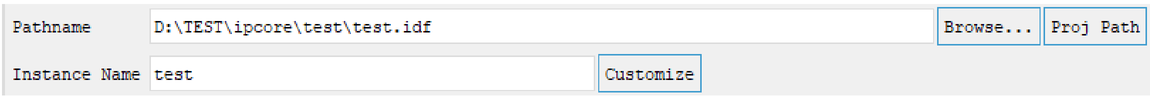


Figure 2-3 Project instantiation interface

2. Configure IP parameter

IP After selecting, click <Customize> to enter 10G MAC+PCS IP Parameter configuration interface. left

Symbol is the interface block diagram, as shown in Figure 2-4 As shown; on the right is the parameter configuration window, as shown in Figure 2-5 shown.

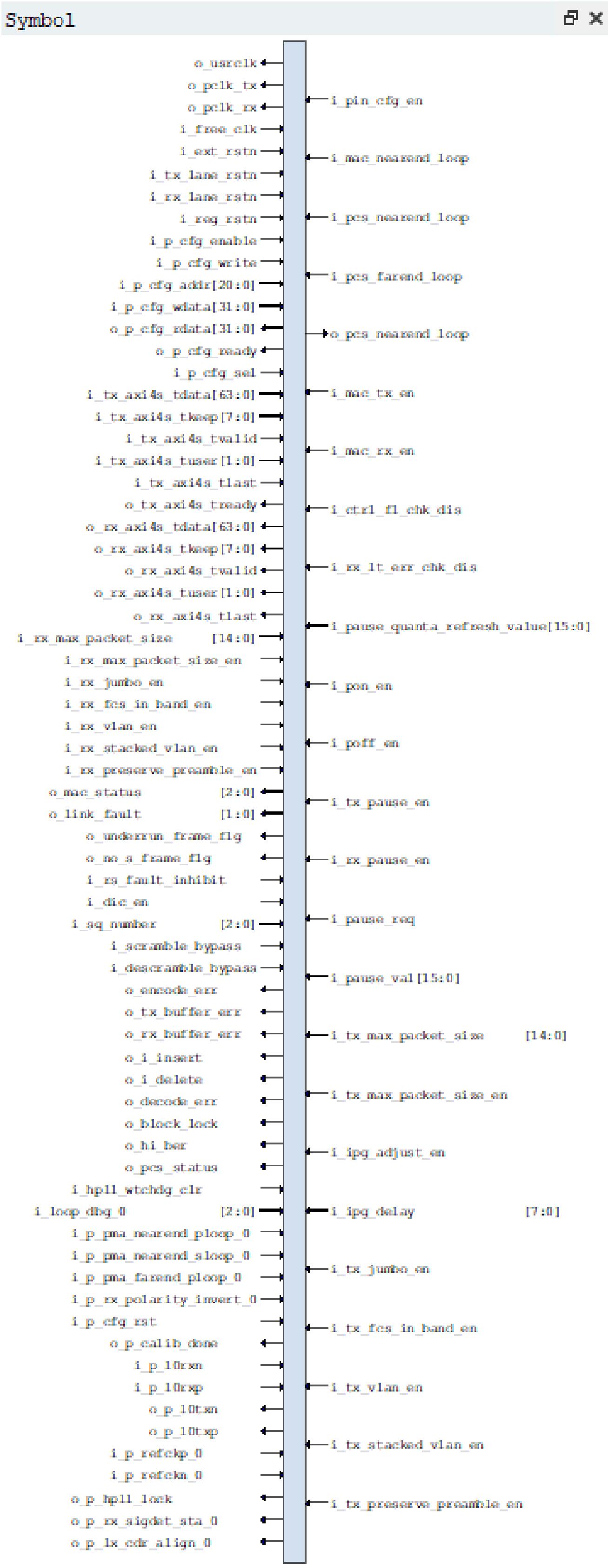


Figure 2-4 10G MAC+PCS IP Interface diagram

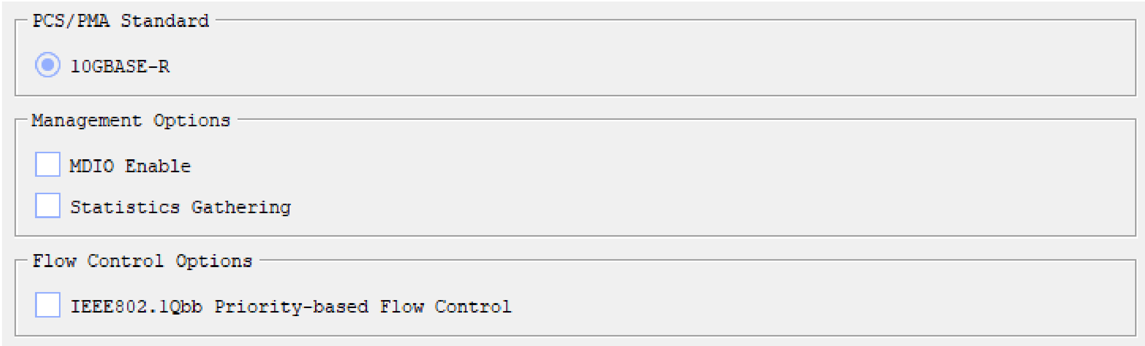


Figure 2-5 10G MAC+PCS IP Configuration parameter interface

Table 2-2 10G MAC+PCS IP Configuration parameter description

Options area	Parameters / configuration options	Parameter Description	IP Configuration interface default value
PCS/PMA Standard	10GBASE- R	10GBASE-R PHY standard	-
Management Options	MDIO Enable	MDIO Configure management interface enable selection Check: enable	Disable
	Statistics Gathering	Statistics Performance statistics collection enable selection Check: enable	Disable
Flow Control Options	IEEE802.1Qbb Priority-based Flow Control	PFC Flow control enable selection Check: enable	Disable

Note: " - " indicates that this parameter is not configurable.

3. Generate IP

After the parameter configuration is completed, click the <Generate> button in the upper left corner to generate the 10G MAC+PCS IP code corresponding to the user- specific settings . The information report interface for generating IP is shown in Figure 2-6 . shown.

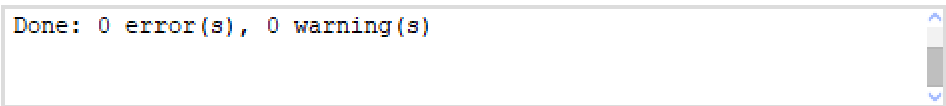


Figure 2-6 10G MAC+PCS IP Generate report interface

Successfully generated IP It will be shown in Figure 2-3 later. Project specified in Output the files shown in the table below under the path.

Table 2-3 10G MAC+PCS IP Generated output file

Output file [1]	illustrate
$instname.v	Generated IP top level.v document.
$instname.idf	Generated IP configuration file.
/rtl/*	Generated IP RTL code file.
/rtl/common/*.v	Generated IP plain text RTL file, this folder stores some common modules.
/rtl/ ipsxe_10gmac_hssthp/	This folder stores HSSTHP IP module.
/rtl/synplify/*.vp	Generated IP non-plaintext RTL file, which is used for synthesis.
/example_design/*	Generated IP Example _ Design Test used Bench , top-level file And some module files used in the design.
/pnr/ core_only/*	Generated IP Check the corresponding project files and pin constraint files.
/pnr/ example_design/*	Generated IP Example _ Design Corresponding project files and pin constraint documents pieces.
/sim/*	Generated IP simulation directory.
/sim_lib/*	Generated IP non-plaintext RTL file, which can be used in ModelSim or VCS simulation.
/rev_1	The default output path of comprehensive reports .(This folder will only be created if the synthesis tool is specified. generate)
readme.txt	readme File describing the IP After generation, the structure of the directory is generated.

Notice:

IP Comes with generated .pds files and .fdc The file is for reference only. Please change the pin constraints according to the actual pin connections when using it.

*.vp *_vpAll.vp in the file File contains other *.vp in the same folder

The contents of the file, selecting this file is equivalent to selecting all other

*.vp file; users can choose to use it according to their own usage habits, but they

cannot be selected at the same time, otherwise an error will be reported.

*_simvpAll.vp Same reason.

constraint configuration

For the specific configuration method of constraint files, you can check PDS Related help documents under the installation path: *User_Constraint_Editor_User_Guide* [5] , *Physical_Constraint_Editor_User_Guide* [6] , *Route_Constraint_Editor_User_Guide* [7] .

Run simulation

10G MAC+PCS IP The simulation is based on Example Design Test _ Bench ongoing. related

1 $instname is the instantiated name entered by the user; "*" is a wildcard character, replacing files of the same type.

Example Design For details, see " 2.4 Example D e si g n ".

About PDS For more detailed information on simulation functions and third-party simulation tools, please refer to PDS Related help documents under the installation path: *Pango_Design_Suite_User Guide* [2] , *Simulation_User_Guide* [4] .

Synthesis and place and route

PDS For specific usage of comprehensive tools and placement and routing tools, please refer to PDS Help documentation in the installation path .

Notice :

with IP Example generated together Design project file .pds and pin constraint file .fdc are stored in the /pnr/example_design directory. The physical constraints need to be modified according to the actual device used and the routing of the PCB board. For details, please refer to " 2.8 Instructions and Precautions ."

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resource utilization

Table 2-4 10G MAC+PCS IP Resource Utilization Typical Values Based on Applicable Devices

device	configuration mode	Resource utilization typical value			
		LUT	**FF**	**USCM**	**HSSTHP**
PG2T390H/ PG2T390HX	default allocation	6625	6615	5	1
	MDIO Enable	6767	6708	6	1
	MDIO Enable Statistics Gathering	7394	7323	6	1
	MDIO Enable Statistics Gathering IEEE802.1Qbb Priority-based Flow Control	8078	7634	6	1

Example Design

This section mainly introduces the 10G- based MAC+PCS IP Example _ Design plan. The program passes two test boards for 10G MAC+PCS IP Send data through HSSTHP Link indication and CRC The verification results, etc. verify whether the data on the receiving side is correct.

Design block diagram

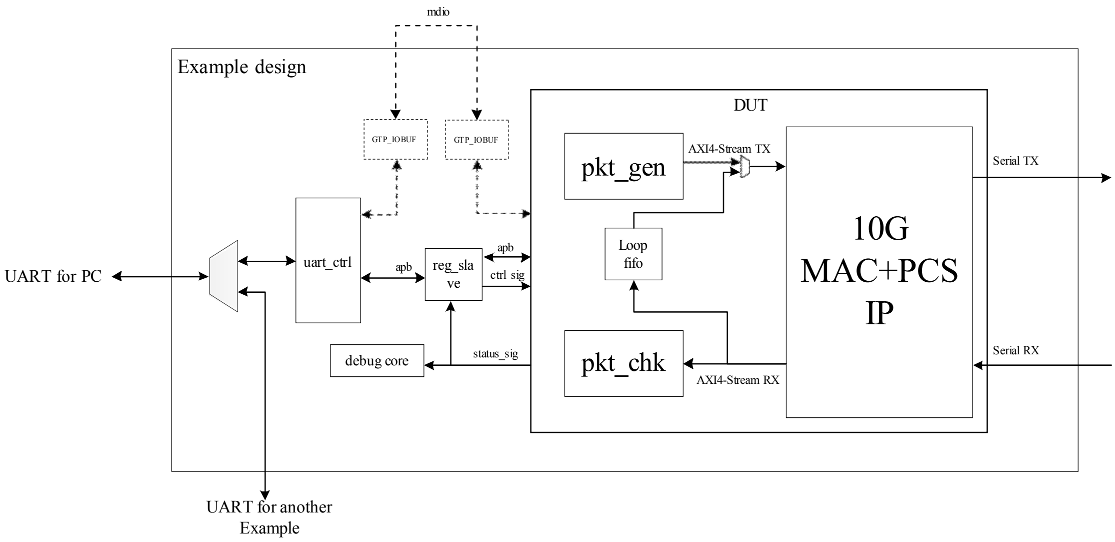


Figure 2-7 Example Design System Block Diagram

Interface Description

Table 2-5 Example Design Interface signal list

port	I/O	bit width	describe	Pin constraints
Clock and reset				
i_free_clk	I	1	External reference clock (50MHz) Used as APB plk _ andHSSTHP _ reset clock	T26
i_ext_rstn	I	1	global reset signal 1 : working normally 0 : reset	T27
MDIO clock and data (MDIO only exists when enabled)				
mdc_10gmac	I	1	MDIO clock input (2MHz)	K30
mdc_uart	O	1	MDIO generated by serial port module clock	M30
mdio_10gmac	IO	1	MDIO data port	L30
mdio_uart	IO	1	MDIO of serial port module data port	N30
UART				
o_txd_a	O	1	UART send data	AF28
i_rxd_a	I	1	UART Receive data	AE28
i_txd_b	I	1	BBoard UART send data	R30
o_rxd_b	O	1	BBoard UART Receive data	U30

i_uart_ctrl_sel	I	1	Current test board selection enable 1 : The current test board is b plate 0 : The current test board is a plate	AK29
port	I/O	bit width	describe	Pin constraints
HSSTHP (HSSTHP dedicated pins)				
i_p_refckp_0	I	1	Reference clock differential input positive terminal (156.25MHz)	G8
i_p_refckn_0	I	1	Reference clock differential input negative terminal (156.25MHz)	G7
i_p_l0rxp	I	1	Channel 0 Differential input positive terminal	K6
i_p_l0rxn	I	1	Channel 0 Differential input negative terminal	K5
o_p_l0txp	O	1	Channel 0 Differential output positive terminal	K2
o_p_l0txn	O	1	Channel 0 Differential output negative terminal	K1
Debug Indicative signal				
o_link_fault	O	1	Link indicator signal 0 : Link is normal 1 : Link abnormality	Y25
o_pcs_status	O	1	Used to indicate PCS_status 1 : block_lock is true and hi_ber is false. 0 : Others.	Y26
o_block_lock	O	1	Instruct PCS BLOCK in SYNC Whether to lock 1 : Locked	AA26
o_hi_ber	O	1	Instruct PCS BER&SYNC in HEADER MONITOR Whether an error SYNC HEADER that exceeds the scope of the protocol is detected 1 : exceed	W27
o_hssthp_hpll_lock	O	1	HSSTHP HPLL _Lock indication signal (asynchronous signal) 1 : Locked 0 : Unlocked	W28
o_p_rx_sigdet_sta_0	O	1	Used to indicate HSSTHP Whether the serial receiving end receives a signal (asynchronous signal) 1 : The signal is normal 0 : signal lost	Y28

port	I/O	bit width	describe	Pin constrain ts
o_p_lx_cdr_align_0	O	1	Used to indicate HSSTHP cdr _Whether to lock (asynchronous signal) 1 : Locked 0 : Unlocked	AA28
o_sfp0_tx_disable	O	1	Optical module TX disable control signal 1 : Disable 0 : Enable	D18

Module description

1. uart_ctrl

Serial port module used during debugging to receive UART data, the baud rate is fixed at 115200 , to APB

Protocol or MDIO The data format required by the protocol is output. The address of read and write operations is 24bit , and the data is 32bit .

(1) Read and write operation instructions

- Read operation format: "address" + " 0 x 72 ".
- Write operation format: "data" + " address" + " 0x77 " .

For related read and write operation examples, please refer to " 2.8.5 uart_ctrl Module read and write operation example ".

2. Address description

via uart_ctrl When the module accesses the register, see Table 2-6 for the address description .

Table 2-6 uart_ctrl Module address description

address bits	illustrate
twenty three	For debugging use only, set to 0 .
twenty two	by APB _Set to 0 when the interface accesses the register ; Via MDIO Set to 1 when interface access register .

twenty one	byAPB _Valid when the interface accesses the register. Set to 0 when accessing the reg_slave module ; Access IP is set to 1 when .
20:0	See " 2.6.4 Register access ".

Notice :

ThisExample _ Design 10G within the project MAC+PCS IP i_hssthp_device_addr _ It is fixed to 0x5 .

3. reg_slave

Custom register module used for debugging, used to view link status and generate some control signals through APB

interface for access. See Table 2-7 for register address description .

Table 2-7 reg_slave Register description

Register address	R/W	describe	default value
0x100014	W	pkg_gen Module packet sending control enable 0x0 : Stop sending packets (default) 0x40000 : Start sending packets	0x0

illustrate:

Use this exampleExample Design The serial port module in accesses reg_slave The register controls when sending packets:

- Start sending packets: write 0x0004000010001477 to the serial port ;
- Stop sending packets: write 0x0000000010001477 to the serial port .

4. debug_core

PDS Comes with own IP for debugging Modules, via Fabric Debugger Tools can realize waveform capture and are used to collect HSSTHP status signal for easy viewing of HSSTHP status. For relevant specific usage, please refer to PDS Help documentation in the installation path.

5. GTP_IOBUF module

Will mdi， mdo Convert to bidirectional IO port MDIO , MDIO only Exists in enable mode.

6. pkg_gen

pkg_gen The module serves as the MAC of the sending end Client， generates the data that needs to be sent based on external control signals.

7. pkt_chk

pkt_chk The module serves as the MAC of the receiving end Client , performs statistics on received data.

8. 10G MAC+PCS IP

10G MAC+PCS IP Top layer, including MAC & PCS and HSSTHP .

Test Methods

InExample _ In the design, users can adjust the 10G MAC+PCS IP is configured via DebugCore and status indication signals to monitor link status for errors. Debug Core See table for signal list 2-8 .

Table 2-8 Debug Core Signal list

DEBUG CORE signal	Engineering signal name	significance
CORE:0 MyFAL0		
TriggerPort0[0]	s_p_rx_sigdet_sta_0	1 : serdes Signal detected
TriggerPort0[1]	s_p_lx_cdr_align_0	1 : CDR OK
TriggerPort0[2]	s_p_hpll_lock	1 : PLL locking
TriggerPort0[3]	s_pcs_status	1 : PCS Normal status
TriggerPort0[4]	s_hi_ber	1 : high appears ber
TriggerPort0[5]	s_block_lock	1 : Synchronization OK
TriggerPort0[6]	tx_buffer_err	1 : TX buffer Occurrence of full
TriggerPort0[7]	rx_buffer_err	1 : RX buffer Occurrence of full
TriggerPort0[255:8]	Missed engineering signal	is 0
CORE:1 MyFAL1		
TriggerPort0[0]	tx_eop	1 : Send end-of-packet indication
TriggerPort0[1]	tx_sop	1 : Send header instructions
TriggerPort0[2]	tx_insert_e	1 : The current frame does not require transmission instructions
TriggerPort0[3]	tx_tvalid	1 : Send data valid indication
TriggerPort0[11:4]	tx_tkeep	Send data control signal 1 : The byte is valid tx_tkeep[0] corresponds to tx_tdata [7:0] (and so on)
TriggerPort0[75:12]	tx_tdata	send data
TriggerPort0[107:76]	tx_pkt_cnt	Send packet statistics
TriggerPort0[139:108]	rx_pkt_cnt	Receive packet statistics

TriggerPort0[171:140]	rx_bad_pkt_cnt	Receive error packet statistics
TriggerPort0[172]	bad_pkt_flg	1 : Error packet indication
TriggerPort0[173]	rx_eop	1 : Receive end-of-packet indication

DEBUG CORE signal	Engineering signal name	significance
TriggerPort0[174]	rx_sop	1 : Receive header indication
TriggerPort0[175]	rx_tvalid	1 : Receive data valid indication
TriggerPort0[183:176]	rx_tkeep	Receive data control signal 1 : The byte is valid rx_tkeep[0] corresponds to tx_tdata [7:0] (and so on)
TriggerPort0[247:184]	rx_tdata	Receive data
TriggerPort0[255:248]	Missed engineering signal	is 0

Take two pieces P05IT2AKF01_A1 (PG2T390H-6FFBG900) Inter-board docking test as an example, through DebugCore Capture data from the sender and receiver (according to Example Design The assignment situation captures the corresponding signal to form a waveform), as shown in Figure 2-8 and Figure 2-9 shown.

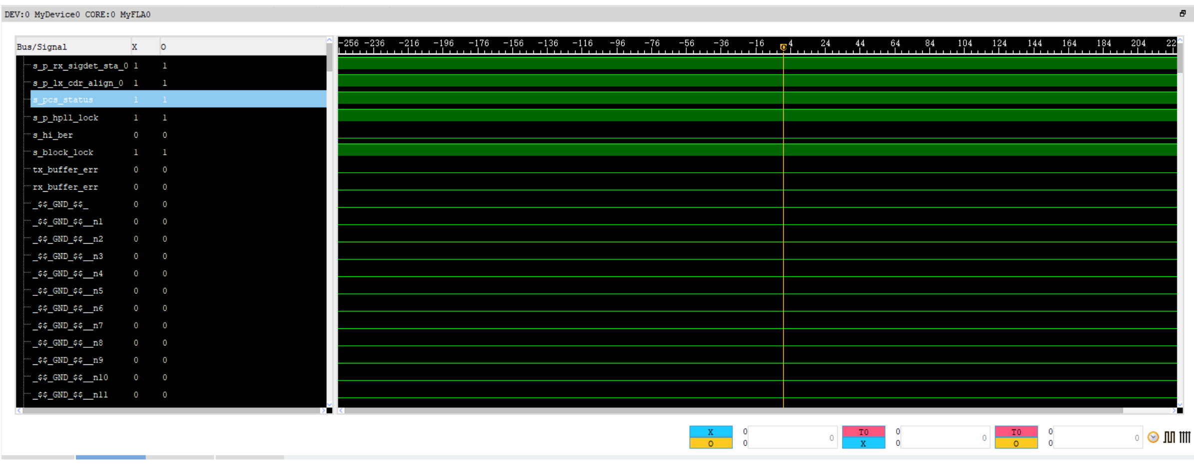


Figure 2-8 Debug Core0 Waveform capture

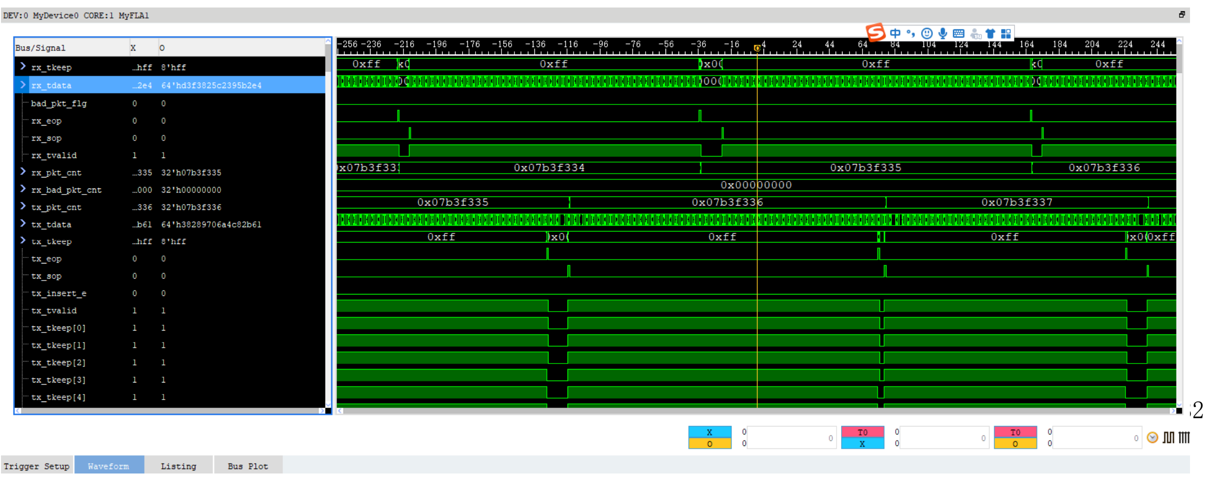


Figure 2-9 Debug Core1 Waveform capture

Instance configuration

Example The choice is MDIO Enable, Statistics Enable and PFC Enabled mode, configuration as shown in Figure 2-10

shown.

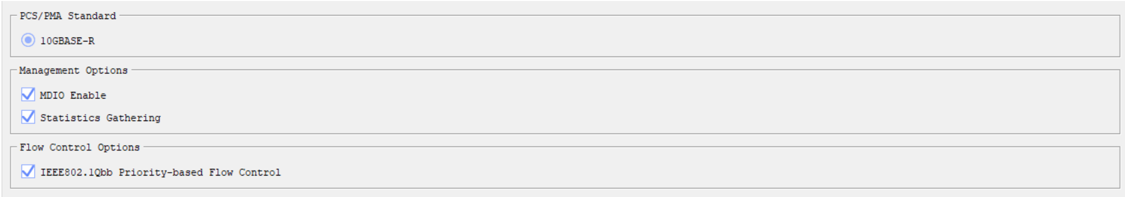


Figure 2-10 Example Configuration diagram

Example simulation

on Windows Under the system, IP After generation, in <project_path>/sim/modelsim Under the path, double-click the *.bat file [2] to run the simulation.

IP Interface description

This section introduces 10G MAC+PCS IP Relevant interface description and timing description.

IP interface description

1. IP interface list

Table 2-9 10G MAC+PCS IP Interface signal list

port	I/O	bit width	describe
Clock and reset			
o_usrclk	O	1	User clock (156.25MHz) as tx and RX direction data transfer clock
o_pclk_tx	O	1	HSSTHP TX _ Clock (161.1328125MHz)
o_pclk_tx	O	1	HSSTHP R X _Clock (161.1328125MHz)
i_free_clk	I	1	HSSTHP IP Reset sequence reference clock (10MHz~100MHz)
i_pclk	I	1	APB clock (30MHz~100MHz)
i_mdc	I	1	MDIO Interface clock signal (up to 2.5MHz)

i_ext_rstn	I	1	global reset signal 1 : reset release 0 : reset
i_tx_lane_rstn	I	1	HSSTHP Tx Lane Soft reset （ i_free_clk clock domain ） 1 : reset release

2 IP See Table 2-3 for the generated output file .

端口	I/O	位宽	描述
			0：复位
i_rx_lane_rstn	I	1	HSSTHP RX Lane 软复位（i_free_clk 时钟域） 1：复位释放 0：复位
i_reg_rstn	I	1	10G MAC+PCS 软核寄存器的复位 1：复位释放 0：复位
i_p_cfg_rst	I	1	HSSTHP 的动态配置接口信号 1：复位 0：复位释放 注：复位后 HSSTHP 的所有寄存器恢复到 Parameter 设置的初始值
i_wtchdg_clr	I	1	看门狗计数器的清零信号（i_free_clk 时钟域） 1：清零
AXI4-Stream TX			
i_tx_axi4s_tdata	I	64	输入数据（传给 MAC）
i_tx_axi4s_tkeep	I	8	输入数据控制信号 1：字节有效 bit[0]对应 i_tx_axi4s_tdata[7:0]（依此类推） 注意：i_tx_axi4s_tkeep 只在包尾时才需要判断，且包尾时有效字节需从低字节开始，其余发包时刻为 8’hff。
i_tx_axi4s_tvalid	I	1	输入数据有效指示 1：数据有效
i_tx_axi4s_tuser	I	2	Bit[0]：帧传输中断指示 1：中断当前帧的传输（MAC 需要 Insert /E/） Bit[1]：输入数据包头指示 1：当前位置是数据包头 注意：bit[0]与 bit[1]不能同时为高。
i_tx_axi4s_tlast	I	1	输入数据包尾指示 1：当前位置是数据包尾
o_tx_axi4s_tready	O	1	输入数据接收指示 1：当前 MAC 可以接收输入数据 0：当前 MAC 不能接收输入数据
AXI4-Stream RX			
o_rx_axi4s_tdata	O	64	输出数据（传输给用户）
o_rx_axi4s_tkeep	O	8	输出数据控制信号 1：字节有效 bit[0]对应 o_rx_axi4s_tdata [7:0]（依此类推）
o_rx_axi4s_tvalid	O	1	输出数据有效指示 1：数据有效
o_rx_axi4s_tuser	O	2	bit[0]输出数据错误指示信号（传输给用户） 1：接收了一个错误包

port	I/O	bit width	describe
			bit[1] outputs the data packet header indication signal (transmitted to the user) 1 : The current position is the data packet header 0 : The current position is not the data packet header
o_rx_axi4s_tlast	O	1	Output end of packet indication 1 : The current position is the end of the data packet
Flow Control Function			
i_pon_en [3] _	I	1	PON enable signal 1 : enable
i_poff_en [3]	I	1	POFF enable signal 1 : enable
PAUSE Flow Control Signals(IEEE802.3)			
i_pause_req [3]	I	1	to link partner Pause request (the local end sends PAUSE) 1 : PASUE frame sending request
i_pause_val [3]	I	16	Pause time (corresponding to pause_time) i_pause_req is 1 Get configuration time parameters from the port.
i_pause_quanta_refresh_value [3]	I	16	PAUSE frame refresh quanta when quanta count When the set value is reached, resend a PAUSE frame. frame
i_tx_pause_en [3]	I	1	Tx PAUSE Flow control mode enable signal 1 : Enable (i_pause_req effective)
i_rx_pause_en [3]	I	1	RX PAUSE Flow control mode enable signal 1 : enable
PFC Flow Control Signals(IEEE802.1Qbb)			
o_rx_pfc_p0_req	O	1	priority 0 Pause sending request (this end suspends sending)
i_rx_pfc_p0_ack	I	1	priority 0 The notification signal of the pause is known and the internal quanta counter starts counting.
o_rx_pfc_p1_req	O	1	priority 1 Pause sending request (this end suspends sending)
i_rx_pfc_p1_ack	I	1	priority 1 The known pause signals the internal quanta counter to start counting.
o_rx_pfc_p2_req	O	1	priority 2 Pause sending request (this end suspends sending)

i_rx_pfc_p2_ack	I	1	priority 2 The notification signal of the pause is known and the internal quanta counter starts counting.
o_rx_pfc_p3_req	O	1	priority 3 Pause sending request (this end suspends sending)
i_rx_pfc_p3_ack	I	1	priority 3 The notification signal of the pause is known and the internal quanta counter starts counting.
o_rx_pfc_p4_req	O	1	priority 4 Pause sending request (this end suspends sending)
i_rx_pfc_p4_ack	I	1	priority 4 The notification signal of the pause is known and the internal quanta counter starts counting.
o_rx_pfc_p5_req	O	1	priority 5 Pause sending request (this end suspends sending)
i_rx_pfc_p5_ack	I	1	priority 5 The notification signal of the pause is known and the internal quanta counter starts counting.
o_rx_pfc_p6_req	O	1	priority 6 Pause sending request (this end suspends sending)

3 Needed in i_pin_cfg_en is 1， the configured port takes effect.

端口	I/O	位宽	描述
i_rx_pfc_p6_ack	I	1	priority 6 已经知道暂停的告知信号 内部 quanta counter 开始计数
o_rx_pfc_p7_req	O	1	priority 7 的暂停发送请求（本端暂停发送）
i_rx_pfc_p7_ack	I	1	priority 7 已经知道暂停的告知信号 内部 quanta counter 开始计数
i_tx_pfc_p0_req[3]	I	1	对 link partner 的 priority 0 的暂停请求（本端发送PFC）
i_tx_pfc_p1_ req[3]	I	1	对 link partner 的 priority 1 的暂停请求（本端发送PFC）
i_tx_pfc_p2_ req[3]	I	1	对 link partner 的 priority 2 的暂停请求（本端发送PFC）
i_tx_pfc_p3_ req[3]	I	1	对 link partner 的 priority 3 的暂停请求（本端发送PFC）
i_tx_pfc_p4_ req[3]	I	1	对 link partner 的 priority 4 的暂停请求（本端发送PFC）
i_tx_pfc_p5_ req[3]	I	1	对 link partner 的 priority 5 的暂停请求（本端发送PFC）
i_tx_pfc_p6_ req[3]	I	1	对 link partner 的 priority 6 的暂停请求（本端发送PFC）
i_tx_pfc_p7_ req[3]	I	1	对 link partner 的 priority 7 的暂停请求（本端发送PFC）
i_pfc_quanta[3]	I	128	PFC 帧的 time_vector bit[15:0]对应 time[0]（依此类推）
i_pfc_quanta_refresh_value[3]	I	128	PFC 帧刷新 quanta 当 quanta count 计满设定值时重新发送一帧PFC bit[15:0]对应 TX Priority 0（依此类推）
i_tx_priority_enable[3]	I	8	PFC 帧的 priority_enable_vector bit[0]对应 time[0]的 enable（依此类推）
i_rx_priority_enable[3]	I	8	RX 端 PFC 上传使能 bit[0]对应 o_rx_pfc_p0_req 高电平时 o_rx_pfc_px_req 才会根据接收的PFC 上传
i_tx_pfc_en[3]	I	1	TX PFC 使能信号
i_rx_pfc_en[3]	I	1	RX PFC 使能信号
APB 接口（工作在 i_pclk 时钟域下）			
i_p_cfg_enable	I	1	APB 接口的访问使能 1：使能
i_p_cfg_write	I	1	APB 接口的读写选择信号 1：写操作 0：读操作
i_p_cfg_addr	I	19	APB 接口读写地址
i_p_cfg_wdata	I	32	APB 接口写数据
o_p_cfg_rdata	O	32	APB 接口读数据
o_p_cfg_ready	O	1	APB 接口的读写 ready 输出 1：数据有效
i_p_cfg_sel	I	1	APB 接口的片选信号（选中后可以进行 APB 数据传输） 1：选中
MDIO 接口（工作在 i_mdc 时钟域下）			
i_mdi	I	1	MDIO 输入数据
i_phy_addr	I	5	PHY 地址配置总线
i_hssthp_device_addr	I	5	HSSTHP 的 device addr

端口	I/O	位宽	描述
			注意：由于PCS reg 占用的 device addr 1 和 3，HSSTHP 的 device addr 请配置为其他值。
o_mdo	O	1	MDIO 输出数据
o_mdo_en	O	1	MDIO 输出数据使能信号
配置接口			
i_pin_cfg_en	I	1	用户配置端口 1：配置端口有效 0：配置端口无效（使用内部寄存器进行模式配置）
i_mac_nearend_loop[3]	I	1	MAC 近端环回使能信号 1：使能 0：不使能
i_pcs_farend_loop[3]	I	1	PCS 远端环回使能信号 1：使能 0：不使能
i_mac_tx_en[3]	I	1	MAC TX 使能信号 1：使能（接收用户数据） 0：不使能（忽略用户数据）
i_mac_rx_en[3]	I	1	MAC RX 使能信号 1：使能（接收PCS RX 数据） 0：不使能（忽略 PCS RX 数据）
i_tx_max_packet_size[3]	I	15	用户自定义 TX 方向最大包长
i_tx_max_packet_size _en[3]	I	1	用户自定义 TX 方向最大包长模式使能信号
i_rx_max_packet_size[3]	I	15	用户自定义 RX 方向最大包长
i_rx_max_packet_size _en[3]	I	1	用户自定义 RX 方向最大包长模式使能信号
i_dic_en[3]	I	1	DIC 的使能信号 1：Start alignment 采用 DIC； 0：Start alignment 采用 insert idle 方式
i_ipg_adjust_en[3]	I	1	帧间隔调节使能 1：帧间隔采用 i_ipg_delay 定义的字节数 0：帧间隔采用最小帧间隔 12bytes
i_ipg_delay[3]	I	8	控制帧间隔字节数（帧间隔调节使能下有效）
i_tx_jumbo_en[3]	I	1	TX 巨帧模式使能信号 1：帧长可超过 802.3 定义最大帧长 0：最大帧长为 802.3 定义最大帧长
i_rx_jumbo_en[3]	I	1	RX 巨帧模式使能信号 1：帧长可超过 802.3 定义最大帧长 0：最大帧长为 802.3 定义最大帧长
i_tx_fcs_in_band_en[3]	I	1	TX FCS in-band 模式使能信号

端口	I/O	位宽	描述
			1：由用户提供的数据包含 FCS 和 PAD 0：IP 内部计算并填充 FCS 和 PAD
i_rx_fcs_in_band_en[3]	I	1	RX FCS in-band 模式使能信号 1：传给用户的数据包含 FCS 和 PAD 0：IP 内部进行 FCS 校验和去除FCS 和 PAD
i_tx_vlan_en[3]	I	1	TX VLAN 模式使能信号 1：使能 0：不使能
i_rx_vlan_en[3]	I	1	RX VLAN 模式使能信号 1：使能 0：不使能
i_tx_stacked_vlan_en[3]	I	1	TX Stacked VLAN 模式使能信号，需在 i_tx_vlan_en 使能下使用 1：使能 0：不使能
i_rx_stacked_vlan_en[3]	I	1	RX Stacked VLAN 模式使能信号，需在 i_rx_vlan_en 使能下使用 1：使能 0：不使能
i_tx_preserve_preamble_en[3]	I	1	客制化 preamble 透传使能 1：发送端用户自己定义 preamble 传给 MAC，接收端 preamble 保留上传给用户； 0：preamble 按协议定义。
i_rx_preserve_preamble_en[3]	I	1	客制化 preamble 透传使能 1：接收端preamble 保留上传给用户 0：preamble 按协议定义
i_rs_fault_inhibit[3]	I	1	RS fault 处理功能关闭信号 1：RS fault 处理关闭，传输 TX 方向的数据，不理会 Sequence ordered set； 0：按协议根据 fault 类型进行处理。
i_ctrl_fl_chk_dis[3]	I	1	控制帧帧长检测关闭信号 1：关闭
i_rx_lt_err_chk_dis[3]	I	1	接收帧帧长/类型错误检查关闭信号 1：关闭
状态接口			
o_p_hpll_lock	O	1	指示 HSSTHP 内 PLL 是否锁定（异步信号） 1：锁定
o_p_rx_sigdet_sta_0	O	1	指示 Serdes lane 串行接收端是否接收到信号（异步信号） 1：信号正常 0：信号丢失
o_p_lx_cdr_align_0	O	1	指示 Serdes lane 的 cdr 是否锁定（高有效、异步信号） 1：锁定
o_block_lock	O	1	指示PCS 中的 BLOCK SYNC 是否锁定

端口	I/O	位宽	描述
			1：锁定
o_hi_ber	O	1	指示PCS 中的 BER&SYNC HEADER MONITOR 是否检测到超过协议规定范围的错误 SYNC HEADER 1：超过
o_pcs_status	O	1	指示PCS_status 1：block_lock is true and hi_ber is false. 0：Others
o_mac_status	O	3	MAC 的 RS 接收 Sequence ordered set 指示各 bit 定义如下： Bit[0]：RS 是否接收到 local fault 1：接收到 local fault sequence ordered sets Bit[1]：RS 是否接收到 remote fault 1：接收到 remote fault sequence ordered sets Bit[2]：RS 是否接收到 link interruption 1：接收到 link interruption sequence ordered sets
o_link_fault	O	2	MAC 的 RS 状态指示： 00：OK(No fault). 01：Local Fault; fault detected by the PHY. 10：Remote Fault; fault detection signaled by the remote RS. 11：Link Interruption; link temporarily unavailable, signaled by the PHY.
o_tx_buffer_err	O	1	指示 10G MAC TX 方向的 afifo 是否空满 1：发生空满
o_rx_buffer_err	O	1	指示 10G MAC RX 方向的 afifo 是否空满 1：发生空满
o_underrun_frame_flg	O	1	指示传输的上一帧尾 underrun error frame underrun error 分为三种情况： 第一种是 i_tx_axi4s_tuser[0]在发送数据时拉高；第二种是 数据传输了但是没有 i_tx_axi4s_last； 第三种是帧长超过限定的最大帧长。
o_no_s_frame_flg	O	1	指示接收到没有/S/的数据帧（被 RS 丢弃） 1：有效
o_encode_err	O	1	64B/66B 编码进入RX_E 指示
o_decode_err	O	1	64B/66B 解码进入RX_E 指示
o_i_insert	O	1	RX BUFFER 插入 idle 指示
o_i_delete	O	1	RX BUFFER 删除 idle 指示
HSSTHP			
i_p_refckp_0	I	1	参考时钟差分输入正端（156.25MHz）
i_p_refckn_0	I	1	参考时钟差分输入负端（156.25MHz）
i_p_l0rxp	I	1	Channel 0 差分输入正端
i_p_l0rxn	I	1	Channel 0 差分输入负端

port	I/O	bit width	describe
o_p_l0txn	O	1	Channel 0 Differential output negative terminal
i_loop_dbg_0	I	3	Please refer to UG051004_Titan2_HSSTHP_IP_UserGuide.pdf
i_p_pma_nearend_ploop_0	I	1	Please refer to UG051004_Titan2_HSSTHP_IP_UserGuide.pdf
i_p_pma_nearend_sloop_0	I	1	Please refer to UG051004_Titan2_HSSTHP_IP_UserGuide.pdf
i_p_pma_farend_ploop_0	I	1	Please refer to UG051004_Titan2_HSSTHP_IP_UserGuide.pdf
i_p_rx_polarity_invert_0	I	1	Please refer to UG051004_Titan2_HSSTHP_IP_UserGuide.pdf
o_p_calib_done	O	1	Please refer to UG051004_Titan2_HSSTHP_IP_UserGuide.pdf

Notice:

PFC andPAUSE _Only one of the two flow control mechanisms can be enabled, and only one of the corresponding interfaces is valid.

Register management interface timing

10G MAC+PCS IP Provides two register configuration management interfaces - APB Interfaces and MDIO interface, configure " MDIO" through the interface Enable "Select whether to enable MDIO interface. For detailed description, please refer to " 2.3.1 2 Configure IP parameters ."

1. APB interface

(1) APB write operation

byAPB _When performing a read operation, first pull p_cfg_sel high Select APB interface, pull p_cfg_enable and p_cfg_write high at the same time , enter the effective address p_cfg_addr Request to write data, lasts 1 Cycle _ Finally, p_cfg_ready is pulled high, valid data is written, and then p_cfg_enbale is pulled low, and a write operation is completed.

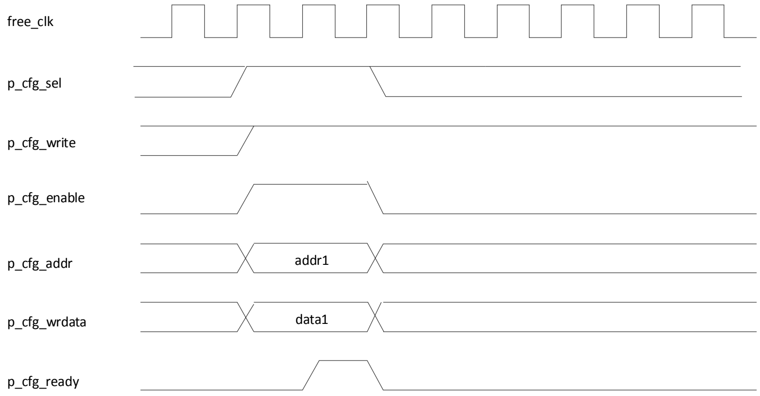


Figure 2-11 APB Write operation timing

(2) APB Read operation

byAPB _ When performing a read operation, first pull p_cfg_sel high Select APB interface, pull p_cfg_enable high and p_cfg_write low at the same time , enter the effective address p_cfg_addr Request to read data, lasting several Cycles Afterwards, p_cfg_ready is pulled high, valid data is read, and then p_cfg_enbale is pulled low, and a read operation is completed.

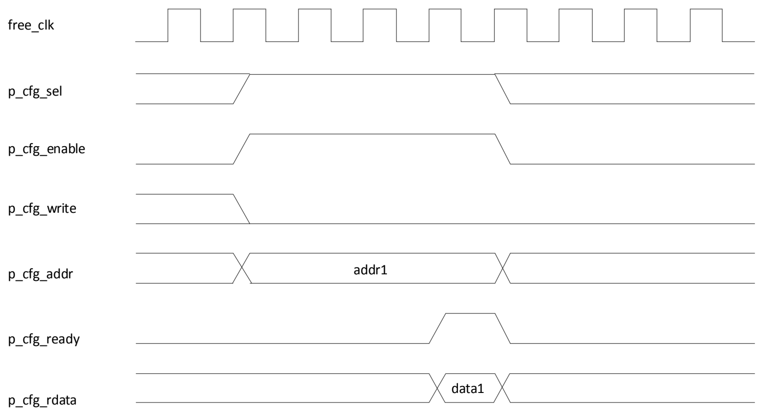


Figure 2-12 APB Read operation timing

2. MDIO interface

(1) write operation

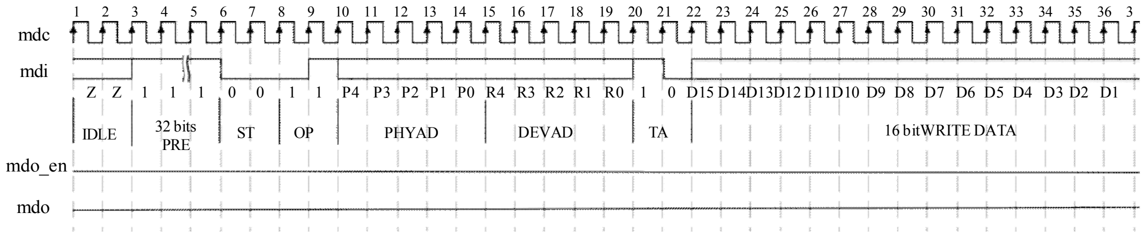


Figure 2-13 MDIO Write operation timing

(2) Read operation

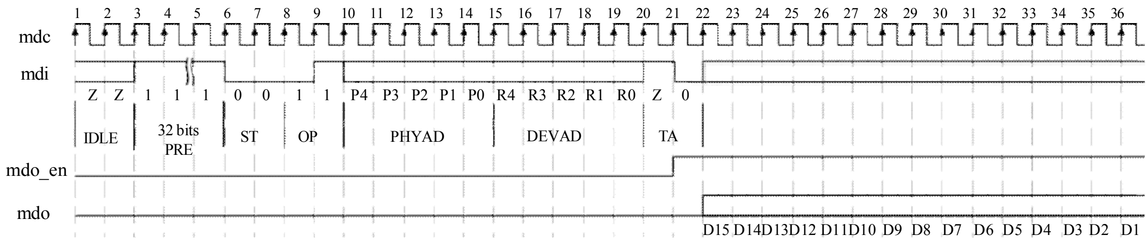


Figure 2-14 MDIO Read operation timing

(3) Address setting

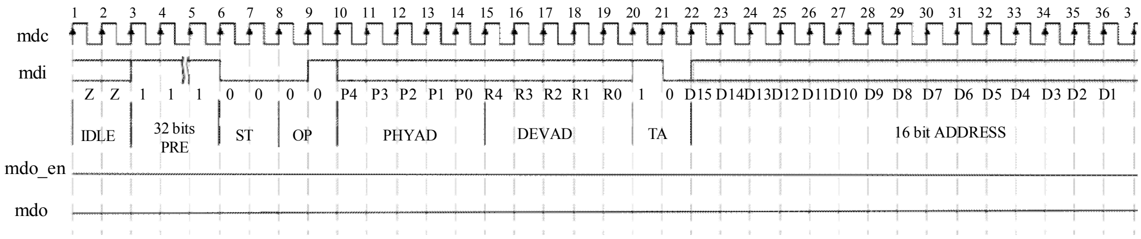


Figure 2-15 MDIO Address setting timing chart

(4) Add address after reading

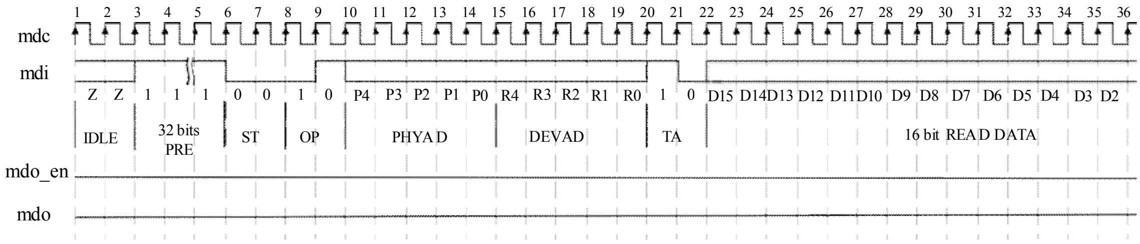


Figure 2-16 MDIO Address self-increment timing after reading

AXI4-Stream Interface timing

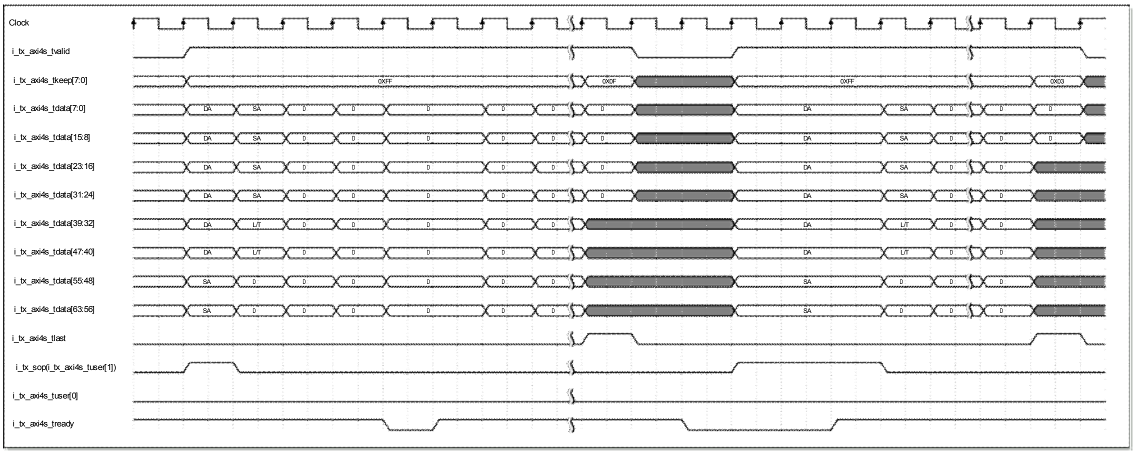


Figure 2-17 AXI4-Stream Tx Interface timing

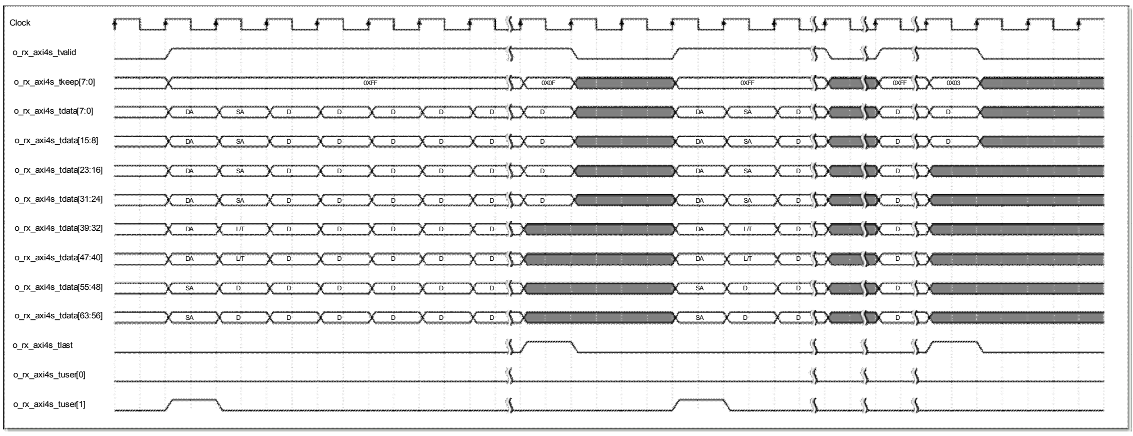


Figure 2-18 AXI4-Stream RX Interface timing

IP Register description

This section introduces 10G MAC+PCS IP Related register descriptions and access methods.

MAC Core Register description

MAC Core Registers include Statistics registers and configuration status registers. Statistics The register is used for data packet information collection; the configuration status register is used for working mode configuration and link status reporting. For information about register access, please refer to " 2.6.4 Register access ".

1. Statistics register

Statistics Register TX The base address is 0x5000 , RX The base address is 0x5800 .

(1) Tx Statistic

Table 2-10 Tx DirectionStatistics _Register list

offset address	register	describe	Attributes	default value
0x0000	Transmitted bytes (LSW)	Statistics of number of bytes sent	RO	0x0
0x0004	Transmitted bytes (MSW)	Statistics of number of bytes sent	RO	0x0
0x0008	64 byte frames transmitted OK (LSW)	The frame length sent is equal to 64 Bytes and correct number of frames Quantitative statistics	RO	0x0
0x000c	64 byte frames transmitted OK (MSW)	The frame length sent is equal to 64 Bytes and correct number of frames Quantitative statistics	RO	0x0
0x0010	65~127 byte frames transmitted OK (LSW)	The frame length sent is between 65~127 Bytes and correct frame Quantity statistics	RO	0x0
0x0014	65~127 byte frames transmitted OK (MSW)	The frame length sent is between 65~127 Bytes and correct frame Quantity statistics	RO	0x0
0x0018	128~255 byte frames transmitted OK (LSW)	The frame length sent is between 128~255 Bytes and correct frame Quantity statistics	RO	0x0
0x001c	128~255 byte frames transmitted OK (MSW)	The frame length sent is between 128~255 Bytes and correct frame Quantity statistics	RO	0x0
0x0020	256~511 byte frames transmitted OK (LSW)	The frame length sent is between 256~511 Bytes and correct frame Quantity statistics	RO	0x0
0x0024	256~511 byte frames transmitted OK (MSW)	The frame length sent is between 256~511 Bytes and correct frame Quantity statistics	RO	0x0

0x0028	512~1023 byte frames transmitted OK (LSW)	The frame length sent is between 512~1023 Bytes and correct Frame count statistics	RO	0x0
0x002c	512~1023 byte frames transmitted OK (MSW)	The frame length sent is between 512~1023 Bytes and correct Frame count statistics	RO	0x0
0x0030	1024~MaxFrameSize byte frames transmitted OK (LSW)	1024 and the maximum frame length bytes sent (according to 802.3 Define the maximum frame Length 1518 byte)	RO	0x0
0x0034	1024~MaxFrameSize byte frames transmitted OK (MSW)	1024 and the maximum frame length bytes sent (according to 802.3 Define the maximum frame Length 1518 byte)	RO	0x0

偏移地址	寄存器	描述	属性	默认值
0x0038	Oversize frames transmitted OK (LSW)	发送的帧长超过最大帧长字节且正确的帧的数量统计（按 802.3 定义最大帧长 1518 字节）	RO	0x0
0x003c	Oversize frames transmitted OK (MSW)	发送的帧长超过最大帧长字节且正确的帧的数量统计（按 802.3 定义最大帧长 1518 字节）	RO	0x0
0x0040	Frames transmitted OK (LSW)	发送的帧无错误的帧的数量统计	RO	0x0
0x0044	Frames transmitted OK (MSW)	发送的帧无错误的帧的数量统计	RO	0x0
0x0048	Broadcast frames transmitted OK (LSW)	发送的帧的目的地址为 Broadcast address 且无错误的帧的数量统计	RO	0x0
0x004c	Broadcast frames transmitted OK (MSW)	发送的帧的目的地址为 Broadcast address 且无错误的帧的数量统计	RO	0x0
0x0050	Multicast frames transmitted OK (LSW)	发送的帧的目的地址为 Multicast address 且无错误的帧的数量统计	RO	0x0
0x0054	Multicast frames transmitted OK (MSW)	发送的帧的目的地址为 Multicast address 且无错误的帧的数量统计	RO	0x0
0x0058	Underrun errors (LSW)	不愿传输的帧或没有包尾的帧或超过最大帧长进行截包处理的帧的数量统计	RO	0x0
0x005c	Underrun errors (MSW)	不愿传输的帧或没有包尾的帧或超过最大帧长进行截包处理的帧的数量统计	RO	0x0
0x0060	Control frames transmitted OK (LSW)	成功传输的控制帧的数量统计	RO	0x0
0x0064	Control frames transmitted OK (MSW)	成功传输的控制帧的数量统计	RO	0x0
0x0068	VLAN tagged frames transmitted OK (LSW)	VLAN 或 stacked vlan 模式下，成功传输的 VLAN 或 stacked vlan tag 帧的数量统计	RO	0x0
0x006c	VLAN tagged frames transmitted OK (MSW)	VLAN 或 stacked vlan 模式下，成功传输的 VLAN 或 stacked vlan tag 帧的数量统计	RO	0x0
0x0070	PAUSE frames transmitted OK (LSW)	成功传输的PAUSE 控制帧的数量统计	RO	0x0
0x0074	PAUSE frames transmitted OK (MSW)	成功传输的PAUSE 控制帧的数量统计	RO	0x0
0x0078	TX Priority Flow Control Frames transmitted OK (LSW)	成功传输的PFC 控制帧的数量统计	RO	0x0
0x007c	TX Priority Flow Control Frames transmitted OK (MSW)	成功传输的PFC 控制帧的数量统计	RO	0x0

(2) **RX Statistic**

Table 2-11 RX DirectionStatistics _Register list

offset address	register	describe	Attributes	default value
0x0000	Received bytes(LSW)	Received byte count statistics	RO	0x0
0x0004	Received bytes(MSW)	Received byte count statistics	RO	0x0
0x0008	Undersize frames received (LSW)	The received frame length is less than 64 bytes, but the FCS is correct Frame count statistics	RO	0x0
0x000c	Undersize frames received (MSW)	The received frame length is less than 64 bytes, but the FCS is correct Frame count statistics	RO	0x0
0x0010	Fragment frames received (LSW)	The received frame length is less than 64 bytes, but FCS is wrong Frame count statistics	RO	0x0
0x0014	Fragment frames received (MSW)	The received frame length is less than 64 bytes, but FCS is wrong Frame count statistics	RO	0x0
0x0018	64 byte frames received OK (LSW)	The received frame length is equal to 64 Bytes and correct number of frames Quantitative statistics	RO	0x0
0x001c	64 byte frames received OK (MSW)	The received frame length is equal to 64 Bytes and correct number of frames Quantitative statistics	RO	0x0
0x0020	65~127 byte frames received OK (LSW)	The received frame length is between 65~127 Bytes and correct frame Quantity statistics	RO	0x0
0x0024	65~127 byte frames received OK (MSW)	The received frame length is between 65~127 Bytes and correct frame Quantity statistics	RO	0x0
0x0028	128~255 byte frames received OK (LSW)	The received frame length is between 128~255 Bytes and correct frame Quantity statistics	RO	0x0
0x002c	128~255 byte frames received OK (MSW)	The received frame length is between 128~255 Bytes and correct frame Quantity statistics	RO	0x0
0x0030	256~511 byte frames received OK (LSW)	The received frame length is between 256~511 Bytes and correct frame Quantity statistics	RO	0x0
0x0034	256~511 byte frames received OK (MSW)	The received frame length is between 256~511 Bytes and correct frame Quantity statistics	RO	0x0
0x0038	512~1023 byte frames received OK (LSW)	The received frame length is between 512~1023 Bytes and correct	RO	0x0

		Frame count statistics		
0x003c	512~1023 byte frames received OK (MSW)	The received frame length is between 512~1023 Bytes and correct Frame count statistics	RO	0x0
0x0040	1024~MaxFrameSize byte frames received OK (LSW)	which the received frame length is between 1024 and the maximum frame length bytes (according to 802.3 Define the maximum frame Length 1518 byte)	RO	0x0
0x0044	1024~MaxFrameSize byte frames received OK (MSW)	which the received frame length is between 1024 and the maximum frame length bytes (according to 802.3 Define the maximum frame Length 1518 byte)	RO	0x0
0x0048	Oversize frames received OK (LSW)	The received frame length exceeds the maximum frame length bytes and is correct Frame number statistics (according to 802.3 Define the maximum frame length	RO	0x0

偏移地址	寄存器	描述	属性	默认值
		1518 字节）		
0x004c	Oversize frames received OK (MSW)	接收的帧长超过最大帧长字节且正确的帧的数量统计（按 802.3 定义最大帧长 1518 字节）	RO	0x0
0x0050	Frames received OK (LSW)	接收的帧无错误的帧的数量统计	RO	0x0
0x0054	Frames received OK (MSW)	接收的帧无错误的帧的数量统计	RO	0x0
0x0058	Frame Check Sequence errors (LSW)	接收的帧出现 FCS 错误的帧的数量统计	RO	0x0
0x005c	Frame Check Sequence errors (MSW)	接收的帧出现 FCS 错误的帧的数量统计	RO	0x0
0x0060	Broadcast frames received OK (LSW)	接收的帧的目的地址为 Broadcast address 且无错误的帧的数量统计	RO	0x0
0x0064	Broadcast frames received OK (MSW)	接收的帧的目的地址为 Broadcast address 且无错误的帧的数量统计	RO	0x0
0x0068	Multicast frames received OK (LSW)	接收的帧的目的地址为 Multicast address 且无错误的帧的数量统计	RO	0x0
0x006c	Multicast frames received OK (MSW)	接收的帧的目的地址为 Multicast address 且无错误的帧的数量统计	RO	0x0
0x0070	Control frames received OK (LSW)	接收的帧为控制帧且无错误的帧的数量统计	RO	0x0
0x0074	Control frames received OK (MSW)	接收的帧为控制帧且无错误的帧的数量统计	RO	0x0
0x0078	Length/Type out of range (LSW)	接收的帧的 Length/Type 和数据长度不一致的帧的数量统计	RO	0x0
0x007c	Length/Type out of range (MSW)	接收的帧的 Length/Type 和数据长度不一致的帧的数量统计	RO	0x0
0x0080	VLAN tagged frames received OK (LSW)	在 VLAN 或 stacked Vlane 模式下，接收的无错误的 VLAN 或 stacked Vlan tag 帧的数量统计	RO	0x0
0x0084	VLAN tagged frames received OK (MSW)	在 VLAN 或 stacked Vlane 模式下，接收的无错误的 VLAN 或 stacked Vlan tag 帧的数量统计	RO	0x0
0x0088	PAUSE frames received OK (LSW)	成功接收的帧为PAUSE 帧的数量统计	RO	0x0
0x008c	PAUSE frames received OK (MSW)	成功接收的帧为PAUSE 帧的数量统计	RO	0x0
0x0090	Control frames received with	接收的帧为控制帧，但不支持的控制帧的数量统计	RO	0x0

offset address	register	describe	Attributes	default value
	with unsupported opcode (MSW)	total		
0x0098	Priority Flow control frames received OK (LSW)	Successfully received frames are PFC Frame count statistics	RO	0x0
0x009c	Priority Flow control frames received OK (MSW)	Successfully received frames are PFC Frame count statistics	RO	0x0

2. Configuration status register

Configure status register TX The direction base address is 0x6000， RX The direction base address is 0x6800 .

(1) Transmit Configuration

Table 2-12 Transmit Configuration Register list

offset address	Bit Bit	register	describe	Attributes	default value
0x0000	[31:17]	Reserved	Reserved	RO	0x0
	[16]	Transmitter Reset	Reset on sending side 1 : Reset	R/W	0
	[15]	Jumbo Frame Enable	Jumbo mode enable 1 : enable After enabling, the sender can send frames exceeding the maximum frame length. frame (by 802.3 Define the maximum frame length 1518 byte)	R/W	0
	[14]	In-band FCS Enable.	FCS Transparent transmission enabled 1 : enable After enabling, the sender will send client Transport FCS Penetrate	R/W	0
	[13]	Transmitter Enable	The sender is enabled. 1 : enable	R/W	1
	[12]	VLAN Enable	VLAN mode enable 1 : enable After enabling VLAN tagged Frames can be sent, maximum The frame length is 1522 byte.	R/W	0

	[11]	Interframe Gap Adjust Enable	Frame interval adjustment enable 1 : enable After enabling, the frame interval adopts i_ipg_delay configuration value Configure the frame interval	R/W	0
	[10]	Deficit Idle Count Enable	DIC Enable 1 : enable start after enabling alignment Using DIC The way	R/W	0

offset address	Bit Bit	register	describe	Attributes	default value
	[9]	Transmitter Preserve Preamble Enable	Preamble transparent transmission enabled 1 : enable preamble after enabling from client	R/W	0
	[8]	Stacked VLAN Mode Enable	stacked VLAN Mode enable, 1 : enabled. make The sender can support stacked VLAN frame	R/W	0
	[7:0]	IPG delay	Frame interval adjustment value	R/W	0xc

(2) Tx Flow Control Configuration

Table 2-13 Tx DirectionFlow _ Control Configuration Register list

offset address	Bit Bit	register	describe	Attributes	default value
0x0004	[31:21]	Reserved	Reserved	RO	0
	[20]	Flow Control Enable (TX)	Tx Directional flow control (PAUSE mode) enabled 1 : enable i_pause_req after enabling is effective	R/W	1
	[19]	Priority pause flow control enable (TX).	Tx Directional Flow Control (PFC mode) enable 1 : enable i_tx_pfc_px_req after enabling is effective	R/W	0
	[18]	Tx Auto PON	1 : open After opening, in i_tx_pfc_px_req on the falling edge of will automatically send a pause time of 0 PFC _ frame, Let the peer TX Data flow recovery	R/W	1
	[17]	Tx Auto POFF	1 : On. After opening, in i_tx_pfc_px_req is high and exceeds When the refresh time expires, the pause time will be automatically sent to 0. P F C _ frame, let the peer TX Data flow recovery	R/W	1
	[16]	PAUSE req	Tx Directional flow control (PAUSE method) pause request	R/W	0
	[15:8]	PFC req	Tx Directional Flow Control (PFC	R/W	0

			method) pause request, bit0 Corresponding to Priority 0, and so on		
	[7]	TX Priority 7 pause enable	Tx Directional Flow Control (PFC mode) enable 1 : enable After enabling, i_tx_pfc_p7_req is effective	R/W	1
	[6]	TX Priority 6 pause enable	Tx Directional Flow Control (PFC mode) enable 1 : enable After enabling, i_tx_pfc_p6_req is effective	R/W	1
	[5]	TX Priority 5 pause enable	Tx Directional Flow Control (PFC mode) enable 1 : enable After enabling, i_tx_pfc_p5_req is effective	R/W	1
	[4]	Tx Priority 4 pause enable	Tx Directional Flow Control (PFC mode) enable 1 : enable	R/W	1

offset address	Bit Bit	register	describe	Attributes	default value
			After enabling, i_tx_pfc_p4_req is effective		
	[3]	TX Priority 3 pause enable	Tx Directional Flow Control (PFC mode) enable 1 : enable After enabling, i_tx_pfc_p3_req is effective	R/W	1
	[2]	TX Priority 2 pause enable	Tx Directional Flow Control (PFC mode) enable 1 : enable After enabling, i_tx_pfc_p2_req is effective	R/W	1
	[1]	TX Priority 1 pause enable	Tx Directional Flow Control (PFC mode) enable 1 : enable After enabling, i_tx_pfc_p1_req is effective	R/W	1
	[0]	TX Priority 0 pause enable	Tx Directional Flow Control (PFC mode) enable 1 : enable After enabling, i_tx_pfc_p0_req is effective	R/W	1

(3) Tx MTU Configuration

Table 2-14 Tx Direction MTU Configuration Register list

offset address	Bit Bit	register	describe	Attributes	default value
0x0008	[31:16]	Reserved	Reserved	RO	0
	[15]	Tx MTU Enable	Tx Maximum frame length configuration enabled 1 : enable After enabling, use the configured value as the maximum frame length.	R/W	0
	[14:0]	Tx MTU Size	Tx Configure the maximum frame length value	R/W	0x05EE

(4) Tx Priority Quanta Configuration

Table 2-15 Tx DirectionPriority _ Quanta Configuration Register list

offset address	Bit Bit	register	describe	Attributes	default value
0x000c	[31:16]	Priority 0 refresh value	Priority 0 PFC _ quanta refresh time On the premise of a pause request , a PFC frame will be resent every set time.	R/W	0xff00
	[15:0]	Priority 0 pause value	Priority 0 PFC _ quanta value	R/W	0xffff
0x0010	[31:16]	Priority 1 refresh value	Priority 1 PFC _ quanta refresh time On the premise of a pause request , a PFC frame will be resent every set time.	R/W	0xff00
	[15:0]	Priority 1 pause value	Priority 1 PFC _ quanta value	R/W	0xffff

offset address	Bit Bit	register	describe	Attributes	default value
0x0014	[31:16]	Priority 2 refresh value	Priority 2 PFC _ quanta refresh time On the premise of a pause request , a PFC frame will be resent every set time.	R/W	0xff00
	[15:0]	Priority 2 pause value	Priority 2 PFC _ quanta value	R/W	0xffff
0x0018	[31:16]	Priority 3 refresh value	Priority 3 PFC _ quanta refresh time On the premise of a pause request , a PFC frame will be resent every set time.	R/W	0xff00
	[15:0]	Priority 3 pause value	Priority 3 PFC _ quanta value	R/W	0xffff
0x001c	[31:16]	Priority 4 refresh value	Priority 4 PFC _ quanta refresh time On the premise of a pause request , a PFC frame will be resent every set time.	R/W	0xff00
	[15:0]	Priority 4 pause value	Priority 4 PFC _ quanta value	R/W	0xffff
0x0020	[31:16]	Priority 5 refresh value	Priority 5 PFC _ quanta refresh time On the premise of a pause request , a PFC frame will be resent every set time.	R/W	0xff00
	[15:0]	Priority 5 pause value	Priority 5 PFC _ quanta value	R/W	0xffff
0x0024	[31:16]	Priority 6 refresh value	Priority 6 PFC _ quanta refresh time On the premise of a pause request , a PFC frame will be resent every set time.	R/W	0xff00
	[15:0]	Priority 6 pause value	Priority 6 PFC _ quanta value	R/W	0xffff
0x0028	[31:16]	Priority 7 refresh value	Priority 7 PFC _ quanta refresh time On the premise of a pause request , a PFC frame will be resent every set time.	R/W	0xff00

	[15:0]	Priority 7 pause value	Priority 7 PFC _ quanta value	R/W	0xffff

(5) Tx PAUSE Quanta Configuration

Table 2-16 Tx directionPAUSE _ Quanta Configuration Register list

offset address	Bit Bit	register	describe	Attributes	default value
0x002c	[31:16]	Pause Quanta refresh value	PAUSE frame quanta refresh time PAUSE frame will be resent every set time .	R/W	0xff00
	[15:0]	Pause quanta	PAUSE quanta value _	R/W	0xffff

(6) Receive Configuration

Table 2-17 Receive Configuration Register list

offset address	Bit Bit	register	describe	Attributes	default value
0x0000	[31:0]	Pause frame MAC address[31:0]	MAC the address of the SA that sends the control frame , the matching address of the DA that receives the control frame , the low byte is transmitted first 4	R/W	0
0x0004	[31:0]	Multi address	DA of received frame multi _ Match address	R/W	0xc200 0001
0x0008	[31:0]	Reserved	Reserved	R/W	0
0x000c	[31:0]	Address	High 16bit f o r M u l t i _ address The high 16bit , Low 16bit for reserved	R/W	0x0180 0000
0x0010	[31:25]	Reserved	Reserved	RO	0
	[twenty four]	Receiver reset	Reset on the receiving side 1 : Reset	R/W	0
	[twenty three]	Jumbo Frame Enable.	Jumbo mode enable 1 : enable After enabling, the receiving end can receive frames exceeding the maximum frame length (according to 802.3 Define the maximum frame length 1518 byte)	R/W	0
	[twenty two]	In-band FCS Enable.	FCS Transparent transmission enabled 1 : enable After enabling, the receiving end will FCS Transparently passed to client	R/W	0
	[twenty one]	Receiver Enable	Receiver enable 1 : enable	R/W	1
	[20]	VLAN Enable	VLAN mode enable 1 : enable After enabling VLAN tagged Frames can be received with a maximum frame length of 1522 bytes	R/W	0
	[19]	Receiver Preserve Preamble Enable	Preamble transparent transmission enabled 1 : enable After enabling, the receiving end	R/W	0

			transparently transmits the preamble to the client.		
	[18]	Length/Type Error Check Disable	Length/Type Check is not enabled 1 : Disabled After disabling it, the receiving end no longer responds to Length/Type Check for errors	R/W	0
	[17]	Control Frame Length Check Disable.	Control frame length check is disabled 1 : Disabled When disabled, the receiving end will not send a frame longer than 64byte The control frame is considered an error frame	R/W	0
	[16]	Stacked VLAN Mode Enable	stacked VLAN mode enable 1 : enable	R/W	0

4 For example MAC The address is AA-BB-CC-DD-EE-FF , then this register needs to be configured as FF-EE-DD-CC-BB-AA .

offset address	Bit Bit	register	describe	Attributes	default value
			After enabling, the receiving end supports stacked VLAN frame		
	[15:0]	Pause frame MAC address [47:32]	MAC the address of SA for sending frames , DA for receiving frames matching address	R/W	0

(7) RX Flow Control Configuration

Table 2-18 RX DirectionFlow _ Control Configuration Register list

offset address	Bit Bit	register	describe	Attributes	default value
0x0014	[31:10]	Reserved	Reserved	RO	0
	[9]	Flow Control Enable (RX)	RX Directional flow control (PAUSE mode) enable 1 : enable After enabling, i_pause_req is effective	R/W	1
	[8]	Priority pause flow control enable (RX)	RX Directional Flow Control (PFC mode) enable 1 : enable After enabling, o_rx_pfc_px_req is effective	R/W	0
	[7]	RX Priority 7 pause enable	RX Directional Flow Control (PFC mode) enable 1 : enable After enabling, o_rx_pfc_p7_req is effective	R/W	1
	[6]	RX Priority 6 pause enable	RX Directional Flow Control (PFC mode) enable 1 : enable After enabling, o_rx_pfc_p6_req is effective	R/W	1
	[5]	RX Priority 5 pause enable	RX Directional Flow Control (PFC mode) enable 1 : enable After enabling, o_rx_pfc_p5_req is effective	R/W	1
	[4]	RX Priority 4 pause enable	RX Directional Flow Control (PFC mode) enable 1 : enable After enabling, o_rx_pfc_p4_req is	R/W	1

			effective		
	[3]	RX Priority 3 pause enable	RX Directional Flow Control （PFC mode） enable 1： enable After enabling， o_rx_pfc_p3_req is effective	R/W	1
	[2]	RX Priority 2 pause enable	RX Directional Flow Control （PFC mode） enable 1： enable After enabling， o_rx_pfc_p2_req is effective	R/W	1
	[1]	RX Priority 1 pause enable	RX Directional Flow Control （PFC mode） enable 1： enable After enabling， o_rx_pfc_p1_req is effective	R/W	1
	[0]	RX Priority 0 pause enable	RX Directional Flow Control （PFC mode） enable 1： enable After enabling， o_rx_pfc_p0_req is effective	R/W	1

(8) RX RS Status

Table 2-19 RX DirectionRS _Status Register list

offset address	Bit Bit	register	describe	Attributes	default value
0x0018	[31:30]	link fault	MAC RS _Status indication, defined as follows: 00： OK; No fault. 01： Local Fault; fault detected by the PHY. 10： Remote Fault; fault detection signaled by the remote RS. 11： Link Interruption; link temporarily unavailable, signaled by the PHY.	RO	0
	[29]	Remote Fault Received	Remote Fault instruct 1 ： RS received remote fault	RC/ LH	0
	[28]	Local Fault Received	Local Fault instruct 1 ： RS received local fault	RC/ LH	0
	[27]	Fault Inhibit	Fault inhibit 1 ： Close fault deal with After closing, receive local fault , remote fault and link After interruption, it will no longer be processed according to the 802.3 protocol.	R/W	0
	[26]	Link Interruption Detected	Link Interruption instruct 1 ： RS Link received Interruption	RC/ LH	0
	[25:0]	Reserved	Reserved	RO	0

(9) RX MTU Configuration

Table 2-20 RX Direction MTU Configuration Register list

offset address	Bit Bit	register	describe	Attributes	default value
0x001c	[31:16]	Reserved	Reserved	RO	0
	[15]	RX MTU Enable	RX Maximum frame length configuration enabled 1 ： enable After enabling, use the configured value as the maximum frame length.	R/W	0
	[14:0]	RX MTU Size	RX Configure the maximum frame length value	R/W	0x05EE

(10) RX addr_mask

Table 2-21 RX Direction addr_mask Register list

offset address	Bit Bit	register	describe	Attributes	default value
0x0020	[31:0]	mac _addr_mask	mac _addr_mask The low 32bit andPause _frame MAC address bit _One-to-one correspondence .	R/W	0
0x0024	[31:0]	addr_mask	[31:16] for mac _addr_mask The high 16bit ; [15:0] is multi_addr_mask The high 16bit ;	R/W	0
0x0028	[31:0]	multi_addr_mask	multi_addr_mask The low 32bit	R/W	0
0x002c	[31:0]	Reserved	Reserved	R/W	0
0x0030	[31:0]	broad_addr_mask_high	[31:16] is reserved [15:0] is multi_addr_mask The high 16bit ;	R/W	0

(11) RX Loopback

Table 2-22 RX DirectionLoopback _Register list

offset address	Bit Bit	register	describe	Attributes	default value
0x0034	[31:8]	Reserved	Reserved	RO	0
	[7]	mac_nearend_loop	1 : Enable MAC near-end loopback	R/W	0
	[6]	Reserved	Reserved	R/W	0
	[5]	pcs_farend_loop	1 : Enable PCS remote loopback	R/W	0
	[4]	addr_err	1 : A frame with a mismatched address was received	RC/LH	0
	[3]	crc_ok	0 : FCS received Error checking frames	RC/LL	1
	[2]	length_err	1 : length received mismatched frames	RC/LH	0
	[1]	frame_too_long	1 : Received a frame larger than the maximum frame length	RC/LH	0
	[0]	frame_too_samll	1 : Less than 64 bytes received frame	RC/LH	0

PCS Register description

PCS The register is mainly used for working mode configuration and link

status reporting, supporting APB and MDIO Two configuration management interfaces , see Table 2-23 for the register list . See " 2.6.4 Register Access" for details on register access .

Table 2-23 10GBASE-R PCS Register list

APB Register address (i_p_cfg_addr[16:1])	MDIO Register address	Register name
0x0	1.0	MDIO Register 1.0: PMA/PMD Control 1
0x2	1.1	MDIO Register 1.1: PMA/PMD Status 1
0x4	1.4	MDIO Register 1.4: PMA/PMD Speed Ability
0x6,0x8	1.5,1.6	MDIO Registers 1.5 and 1.6: PMA/PMD Devices in Package
0xa	1.7	MEDIUM Register 1.7: 10G PMA/PMD Control two
0xc	1.8	MEDIUM Register 1.8: 10G PMA/PMD Status two
0xe	1.9	MDIO Register 1.9: 10G PMD Transmit Disable
0x10	1.10	MDIO Register 1.10: 10G PMD Signal Receive OK
-	1.11 to 1.65535	Reserved
0x12	3.0	MDIO Register 3.0: PCS Control 1
0x14	3.1	MDIO Register 3.1: PCS Status 1
0x16	3.4	MDIO Register 3.4: PCS Speed Ability
0x18,0x1a	3.5,3.6	MDIO Registers 3.5 and 3.6: PCS Devices in Package
0x1c	3.7	MDIO Register 3.7: 10G PCS Control 2
0x1e	3.8	MDIO Register 3.8: 10G PCS Status 2
-	3.9 to 3.31	Reserved
0x20	3.32	MDIO Register 3.32: 10GBASE-R Status 1
0x22	3.33	MDIO Register 3.33: 10GBASE-R Status 2
0x24,0x26,0x28,0x2a	3.34-37	MDIO Register 3.34–37: 10GBASE-R Test Pattern Seed A0–3
0x2c,0x2e,0x30,0x32	3.38-41	MDIO Register 3.38–41: 10GBASE-R Test Pattern Seed B0–3
0x34	3.42	MDIO Register 3.42: 10GBASE-R Test Pattern Control
0x36	3.43	MDIO Register 3.43: 10GBASE-R Test Pattern Error Counter
-	3.44 to 3.65519	Reserved
-	3.65520 to 3.65534	Reserved
0x38	3.65535	MDIO Register 3.65535: 125 Microsecond Timer Control

Note: ″ - ″ means there is no corresponding register.

1. PMA/PMD Control 1

Table 2-24 PMA/PMD Control 1

Bit Bit	register	describe	Attributes	default value
1.0.15	Reserved	Reserved	RO	0
1.0.14	Reserved	Reserved	RO	0
1.0.13	Speed selection (LSB)	1.0.6 1.0.13 1 1 = bits 5:2 select speed 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	RO	1
1.0.12	Reserved	Reserved	RO	0
1.0.11	Reserved	Reserved	RO	0
1.0.10:7	Reserved	Reserved	RO	0
1.0.6	Speed selection (MSB)	1.0.6 1.0.13 1 1 = bits 5:2 select speed 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	RO	1
1.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 x = Reserved 1 0 0 1 = 400 Gb/s 1 0 0 0 = 200 Gb/s 0 1 1 1 = 5 Gb/s 0 1 1 0 = 2.5 Gb/s 0 1 0 1 = Reserved 0 1 0 0 = 25 Gb/s 0 0 1 1 = 100 Gb/s 0 0 1 0 = 40 Gb/s 0 0 0 1 = 10PASS-TS/2BASE- TL 0 0 0 0 = 10 Gb/s	RO	0
1.0.1	Reserved	Reserved(The agreement is defined as PMA Remote loopback , this function is in HSSTHP internally completed, meaningless here)	RO	0
1.0.0	Reserved	Reserved(The agreement is defined as PMA proximal ring Back, this function is in HSSTHP Completed internally, meaningless here)	RO	0

2. PMA/PMD Status 1

Table 2-25 PMA/PMD Status 1

Bit Bit	register	describe	Attributes	default value
1.1.15:8	Reserved	Reserved	RO	0
1.1.7	Local Fault	1 = Local Fault detected	RO	0
1.1.6:3	Reserved	Reserved	RO	0
1.1.2	Receive Link Status	1 = Receive Link UP	RO/ LL	1
1.1.1	Power down ability	fixed to 1	RO	1
1.1.0	Reserved	Reserved	RO	0

3. PMA/PMD Speed Ability

Table 2-26 PMA/PMD Speed Ability

Bit Bit	register	describe	Attributes	default value
1.4.15:1	Reserved	Reserved	RO	0
1.4.0	10G capable	1 = PMA/PMD is capable of operating at 10 Gb/s 0 = PMA/PMD is not capable of operating at 10 Gb/s	RO	1

4. PMA/PMD Devices in Package

Table 2-27 PMA/PMD Devices in Package

Bit Bit	register	describe	Attributes	default value
1.6.15	Vendor- specific Device 2 Present	1 = Vendor-specific device 2 present in package 0 = Vendor-specific device 2 not present in package	RO	0
1.6.14	Vendor-specific device 1present	1 = Vendor-specific device 1 present in package 0 = Vendor-specific device 1 not present in package	RO	0

1.6.13	Reserved	Reserved	RO	0
1.6.12:0	Reserved	Reserved	RO	0
1.5.15:6	Reserved	Reserved	RO	0

Bit Bit	register	describe	Attributes	default value
1.5.5	DTE XS present	1 = DTE XS present in package 0 = DTE XS not present in package	RO	0
1.5.4	PHY XS present	1 = PHY XS present in package 0 = PHY XS not present in package	RO	0
1.5.3	PCS present	1 = PCS present in package 0 = PCS not present in package	RO	1
1.5.2	WIS present	1 = WIS present in package 0 = WIS not present in package	RO	0
1.5.1	PMD/PMA present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO	1
1.5.0	Clause 22 registers present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO	0

5. 10G PMA/PMD Control 2

Table 2-28 PMA/PMD Control 2

Bit Bit	register	describe	Attributes	default value
1.7.15:4	Reserved	Reserved	RO	0
1.7.3:0	PMA/PMD Type Selection	10GBASE- R	RO	0x5

6. 10G PMA/PMD Status 2

Table 2-29 PMA/PMD Status 2

Bit Bit	register	describe	Attributes	default value
1.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO	0x2

1.8.13	Transmit Local Fault Ability	1 = PMA/PMD has the ability to detect a fault condition on the transmit path 0 = PMA/PMD does not have the ability to detect a fault condition on the transmit path	RO	0
1.8.12	Receive Local Fault	1 = PMA/PMD has the ability to detect a fault condition on the	RO	0

Bit 位	寄存器	描述	属性	默认值
	Ability	receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path		
1.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO	0
1.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO	0
1.8.9	Extended abilities	1 = PMA/PMD has extended abilities listed in register 1.11 0 = PMA/PMD does not have extended abilities	RO	0
1.8.8	PMD transmit disable ability	1 = PMD has the ability to disable the transmit path 0 = PMD does not have the ability to disable the transmit path	RO	0
1.8.7	10GBASE-SR ability	1 = PMA/PMD is able to perform 10GBASE-SR 0 = PMA/PMD is not able to perform 10GBASE-SR	RO	0
1.8.6	10GBASE-LR ability	1 = PMA/PMD is able to perform 10GBASE-LR 0 = PMA/PMD is not able to perform 10GBASE-LR	RO	0
1.8.4	10GBASE-LX4 ability	1 = PMA/PMD is able to perform 10GBASE-LX4 0 = PMA/PMD is not able to perform 10GBASE-LX4	RO	0
1.8.3	10GBASE-SW ability	1 = PMA/PMD is able to perform 10GBASE-SW 0 = PMA/PMD is not able to perform 10GBASE-SW	RO	0
1.8.2	10GBASE-LW ability	1 = PMA/PMD is able to perform 10GBASE-LW 0 = PMA/PMD is not able to perform 10GBASE-LW	RO	0
1.8.1	10GBASE-EW ability	1 = PMA/PMD is able to perform 10GBASE-EW 0 = PMA/PMD is not able to perform 10GBASE-EW	RO	0
1.8.0	PMA local loopback ability	1 = PMA has the ability to perform a local loopback function 0 = PMA does not have the ability to perform a local loopback function	RO	1

7. 10G PMD Transmit Disable

Table 2-30 PMD Transmit Disable

Bit Bit	register	describe	Attributes	default value
1.9.15:1	Reserved	Reserved	RO	0
1.9.0	Global PMD transmit disable	1 = Disable transmitter output 0 = Enable transmitter output	RO	0

8. 10G PMD Signal Receive OK

Table 2-31 PMD Signal Receive OK

Bit Bit	register	describe	Attributes	default value
1.10.15:1	Reserved	Reserved	RO	0
1.10.0（generation code note）	Global PMD receive signal detect	1 = Signal detected on receive 0 = Signal not detected on receive	RO	0

9. PCS Control 1

Table 2-32 PCS Control 1

Bit Bit	register	describe	Attributes	default value
3.0.15	Reset	1 = block reset 0 = Normal operation	R/W SC	0
3.0.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W	0
3.0.13	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	RO	1
3.0.12	Reserved	Reserved	RO	0
3.0.11	Reserved	Reserved	RO	0
3.0.10:7	Reserved	Reserved	RO	0

3.0.6	Speed selection	13 6 1 1 = bits 5:2 select speed 0x _ = unspecified x 0 = unspecified	RO	1
3.0.5:2	Speed selection	5 4 3 2 1 1xx = Reserved	RO	0

Bit Bit	register	describe	Attributes	default value
		1 0 1 1 = Reserved 1 0 1 0 = 400 Gb/s 1 0 0 1 = 200 Gb/s 1 0 0 0 = 5 Gb/s 0 1 1 1 = 2.5 Gb/s 0 1 1 0 = Reserved 0 1 0 1 = 25 Gb/s 0 1 0 0 = 100 Gb/s 0 0 1 1 = 40 Gb/s 0 0 1 0 = 10/1 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s		
3.0.1:0	Reserved	Reserved	RO	0

10. PCS Status 1

Table 2-33 PCS Status 1

Bit Bit	register	describe	Attributes	default value
3.1.15:8	Reserved	Reserved	RO	0
3.1.7	Local Fault	1 = Local Fault detected	RO	0
3.1.6:3	Reserved	Reserved	RO	0
3.1.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL	0
3.1.1	Power Down Ability	1 = PCS supports low-power mode 0 = PCS does not support low-power mode	RO	0
3.1.0	Reserved	Reserved	RO	0

11. PCS Speed Ability

Table 2-34 PCS Speed Ability

Bit Bit	register	describe	Attributes	default value
3.4.15:1	Reserved	Reserved	RO	0

3.4.0	10G Capable	1 = PCS is capable of operating at 10 Gb/s 0 = PCS is not capable of operating at 10 Gb/s	RO	1

12. PCS Devices in Package

Table 2-35 PCS Devices in Package

Bit Bit	register	describe	Attributes	default value
3.6.15	Vendor- specific Device 2 Present	1 = Vendor-specific device 2 present in package 0 = Vendor-specific device 2 not present in package	RO	0
3.6.14	Vendor-specific device 1present	1 = Vendor-specific device 1 present in package 0 = Vendor-specific device 1 not present in package	RO	0
3.6.13	Reserved	Reserved	RO	0
3.6.12:0	Reserved	Reserved	RO	0
3.5.15:6	Reserved	Reserved	RO	0
3.5.5	DTE XS present	1 = DTE XS present in package 0 = DTE XS not present in package	RO	0
3.5.4	PHY XS present	1 = PHY XS present in package 0 = PHY XS not present in package	RO	0
3.5.3	PCS present	1 = PCS present in package 0 = PCS not present in package	RO	1
3.5.2	WIS present	1 = WIS present in package 0 = WIS not present in package	RO	0
3.5.1	PMD/PMA present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO	1
3.5.0	Clause 22 registers present	1 = Clause 22 registers present in package 0 = Clause twenty two registers not present in package	RO	0

13. 10G PCS Control 2

Table 2-36 10G PCS Control 2

Bit Bit	register	describe	Attributes	default value
3.7.15:4	Reserved	Reserved	RO	0
3.7.3:0	PCS type selection	10GBASE- R	RO	0

14. 10G PCS Status 2

Table 2-37 PCS Status 2

Bit Bit	register	describe	Attributes	默认值
3.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO	0x2
3.8.13:12	Reserved	Reserved	RO	0
3.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/ LH	0
3.8.10	Receive fault	1 = Fault condition on the receive path 0 = No fault condition on the receive path	RO/ LH	0
3.8.9:3	Reserved	Reserved	RO	0
3.8.2	10GBASE-W capable	1 = PCS is able to support 10GBASE-W PCS type 0 = PCS is not able to support 10GBASE-W PCS type	RO	0
3.8.1	10GBASE-X capable	1 = PCS is able to support 10GBASE-X PCS type 0 = PCS is not able to support 10GBASE-X PCS type	RO	0
3.8.0	10GBASE-R capable	1 = PCS is able to support 10GBASE-R PCS types 0 = PCS is not able to support 10GBASE-R PCS types	RO	1

15. 10GBASE-R Status 1

Table 2-38 10GBASE-R Status 1

Bit Bit	register	describe	Attributes	default value
3.32.15:13	Reserved	Reserved	RO	0

3.32.12	10GBASE-R Link Status	1 = BASE-R or any MultiGBASE-T PCS receive link up 0 = BASE-R or any MultiGBASE-T PCS receive link down	RO	0

Bit Bit	register	describe	Attributes	default value
3.32.11:4	Reserved	Reserved	RO	0
3.32.3	10GBASE-R PRBS9 pattern testing ability	1 = PCS is able to support PRBS9 pattern testing 0 = PCS is not able to support PRBS9 pattern testing	RO	1
3.32.2	10GBASE-R PRBS31 pattern testing ability	1 = PCS is able to support PRBS31 pattern testing 0 = PCS is not able to support PRBS31 pattern testing	RO	1
3.32.1	Hi BER	1 = BASE-R PCS reporting a high BER 0 = BASE-R PCS not reporting a high BER	RO	0
3.32.0	BASE-R PCS block lock	1 = BASE-R or any MultiGBASE-T PCS locked to received blocks 0 = BASE-R or any MultiGBASE-T PCS not locked to received blocks	RO	0

16. 10GBASE-R Status 2

Table 2-39 10GBASE-R Status 2

Bit Bit	register	describe	Attributes	default value
3.33.15	Latched block lock	1 = BASE-R PCS has block lock 0 = BASE-R PCS does not have block lock	RO/LL	0
3.33.14	Latched high BER	1 = BASE-R PCS has reported a high BER 0 = BASE-R PCS has not reported a high BER	RO/LH	0
3.33.13:8	BER	BER counter	RO/NR/RC	0
3.33.7:0	Errored blocks	Errored blocks counter	RO/NR/RC	0

17. 10GBASE-R Test Pattern Seed A0–3

Table 2-40 10GBASE-R Test Pattern Seed A0–3

Bit Bit	register	describe	Attributes	default value
3.37.15:10	Reserved	Reserved	RO	0
3.37.9:0	Test pattern seed A 3	Test pattern seed A bits 48-57	R/W	0
3.36.15:0	Test pattern seed A 2	Test pattern seed A bits 32-47	R/W	0
3.35.15:0	Test pattern seed A 1	Test pattern seed A bits 16-31	R/W	0
3.34.15:0	Test pattern seed A 0	Test pattern seed A bits 0-15	R/W	0

18. 10GBASE-R Test Pattern Seed B0–3

Table 2-41 10GBASE-R Test Pattern Seed B0–3

Bit Bit	register	describe	Attributes	default value
3.41.15:10	Reserved	Reserved	RO	0
3.41.9:0	Test pattern seed B 3	Test pattern seed B bits 48-57	R/W	0
3.40.15:0	Test pattern seed B 2	Test pattern seed B bits 32-47	R/W	0
3.39.15:0	Test pattern seed B 1	Test pattern seed B bits 16-31	R/W	0
3.38.15:0	Test pattern seed B 0	Test pattern seed B bits 0-15	R/W	0

19. 10GBASE-R Test Pattern Control

Table 2-42 10GBASE-R Test Pattern Control

Bit Bit	register	describe	Attributes	default value
3.42.15:7	Reserved	Reserved	RO	0

3.42.6	Single Lane PHY BASE- R PRBS9 transmit test-pattern enable	1 = Enable PRBS9 test-pattern mode on the transmit path 0 = Disable PRBS9 test-pattern mode on the transmit path	R/W	0

Bit Bit	register	describe	Attributes	default value
3.42.5	Single Lane PHY BASE-R PRBS31 receive test-pattern enable	1 = Enable PRBS31 test-pattern mode on the receive path 0 = Disable PRBS31 test-pattern mode on the receive path PS：PRBS31 功能位于 HSSTHP，此寄存器无作用	R/W	0
3.42.4	Single Lane PHY BASE-R PRBS31 transmit test-pattern enable	1 = Enable PRBS31 test-pattern mode on the transmit path 0 = Disable PRBS31 test-pattern mode on the transmit path PS： PRBS31 Function is located in HSSTHP， please send Register has no effect	R/W	0
3.42.3	Transmit test-pattern enable	1 = Enable transmit test pattern 0 = Disable transmit test pattern	R/W	0
3.42.2	Receive test-pattern enable	1 = Enable receive test-pattern testing 0 = Disable receive test-pattern testing	R/W	0
3.42.1	Test-pattern select	1 = Square wave test pattern 0 = Pseudo random test pattern	R/W	0
3.42.0	Data pattern select	1 = Zeros data pattern 0 = LF data pattern	R/W	0

20. 10GBASE-R Test Pattern Error Counter

表 2-43 10GBASE-R Test Pattern Error Counter

Bit Bit	register	describe	Attributes	default value
3.43.15:0	Test- pattern error counter	Error counter	RO/RC	0

21. 125 Microsecond Timer Control

Table 2-44 125 Microsecond Timer Control

Bit Bit	register	describe	Attributes	default value
3.65535.15:0	125 µs timer control	BER monitor module requires 125us for examine.	R/W	0x4ead

HSSTHP IP Register description

HSSTHP IP For register description, please refer to " *UG050008_Titan2* Series *FPGA* High speed serial transceiver (*HSSTHP*) User Guide [8] and UG051004_Titan2_HSSTHP_IP_UserGuide [9] .

Register access

10G MAC+PCS IP Provides two register configuration management interfaces - APB Interfaces and MDIO interface. Configuring " MDIO" via the interface Enable "Select whether to enable MDIO interface. For detailed description, please refer to " 2.3.1 2 Configure IP parameters ."

- MDIO When the interface is enabled, 10G MAC+PCS IP Via MDIO Interface operation HSSTHP IP and PCS

  register, through APB Interface operation MAC Core register.
- MDIO When the interface is disabled, 10G MAC+PCS IP byAPB _ Interface operation HSSTHP IP , PCS

  and MAC Core register.

1. MDIO The interface is not enabled

If MDIO is configured When the interface is disabled, 10G MAC+PCS IP byAPB _ Interface to HSSTHP IP , PCS and MAC Core registers to operate. APB corresponding to different registers For the interface address and data mapping relationship , see Table 2-45 .

Table 2-45 APB Address data mapping table (MDIO disable)

i_p_cfg_addr[20:18]	register	APB Bus address / data mapping
100	MAC Core register	i_p_cfg_addr[17:2] i_p_cfg_wdata[31:0] o_p_cfg_rdata[31:0]
010	PCS register	i_p_cfg_addr[16:1] i_p_cfg_wdata[15:0] o_p_cfg_rdata[15:0]

001	HSSTHP IP register	i_p_cfg_addr[15:0] i_p_cfg_wdata[7:0] o_p_cfg_rdata[7:0]

(1) HSSTHP IP Register access

When i_p_cfg_addr[20:18]=001 When operating HSSTHP IP register.

- i_p_cfg_addr[15:0] is HSSTHP IP The effective address of the register;
- i_p_cfg_rdata[7:0] and i_p_cfg_wdata[7:0] are HSSTHP IP Register valid data;

(2) PCS Register access

When i_p_cfg_addr[20:18]=010 When operating PCS register.

- i_p_cfg_addr[16:1] is PCS The effective address of the register;
- i_p_cfg_rdata[15:0] and i_p_cfg_wdata[15:0] are PCS Valid data in the register;

(3) MAC Core Register access

When i_p_cfg_addr[20:18]=100 When, the operation reads and writes MAC Core register.

- i_p_cfg_addr[17:2] is MAC Core The effective address of the register;
- i_p_cfg_rdata[31:0] and i_p_cfg_wdata[31:0] are MAC Core Register valid data.

2. MDIO Interface enable

If MDIO is configured Interface enable, 10G MAC+PCS IP Via MDIO Interface access HSSTHP IP and PCS

register , through APB Interface access MAC Core register.

(1) HSSTHP IP Register access

HSSTHP Registers and PCS Register shared i_phy_addr Configure PRTAD . Users need to pass i_hssthp_device_addr Port to HSSTHP Make a device addr settings, at this time the user reads and writes HSSTHP through MDIO DEVAD corresponding to the register Need and port i_hssthp_device_addr be consistent. Since the PCS register has occupied 0x1 and 0x3 , the user needs to configure i_hssthp_device_addr to other values.

(2) PCS Register access

MDIO Interface enable, 10G MAC+PCS IP Via MDIO Interface operation PCS register.

(3) MAC Core Register access

MDIO Interface enable, 10G MAC+PCS IP byAPB _ Interface operation PCS register.

typical application

10G MAC+PCS IP For typical applications, please refer to ″ 2.4 Example Design ”.

Instructions and Notes

Clock constraints

In the generated Example Design Engineering constraint file ipsxe_10gmac.fdc , HSSTHP has been IP

The output clock is bound to the global clock. TakeExample _ Design Project example:

```
define_attribute {t:ipsxe_10gmac_dut_v1_0_u0.U_ipsxe_10gmac_inst00.ipm2t_10gmac_hssthp_u0.o_p_refck2core_0} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}
define_attribute {t:ipsxe_10gmac_dut_v1_0_u0.U_ipsxe_10gmac_inst00.ipm2t_10gmac_hssthp_u0.o_p_clk2core_tx_0} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}
define_attribute {t:ipsxe_10gmac_dut_v1_0_u0.U_ipsxe_10gmac_inst00.ipm2t_10gmac_hssthp_u0.o_p_clk2core_rx_0} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}
```

physical constraints

In the generated Example Design Engineering constraint file ipsxe_10gmac.fdc in, HSSTHP has been IP

Serdes _ Channel and reference clock input locations are physically constrained. TakeExample _ Design For example:

```
define_attribute {p:i_p_refckp_0} {PAP_IO_LOC} {G8}
define_attribute {p:i_p_refckn_0} {PAP_IO_LOC} {G7}
define_attribute {i:ipsxe_10gmac_dut_v1_0_u0.U_ipsxe_10gmac_inst00.ipm2t_10gmac_hssthp_u0.U_GTP_HSSTHP_WRAPPER.CHANNEL0_ENABLE.U_LANE0_WRAP.U_LANE0} {PAP_LOC} {HSSTHP_664_1530:U0_HSSTHP_LANE}
define_attribute {i:ipsxe_10gmac_dut_v1_0_u0.U_ipsxe_10gmac_inst00.ipm2t_10gmac_hssthp_u0.U_GTP_HSSTHP_WRAPPER.HPLL_ENABLE.U_HPLL_WRAP.U_HPLL} {PAP_LOC} {HSSTHP_664_1530:U_HSSTHP_COMMON}
```

Users can refer to " *UG051004_Titan2_HSSTHP_IP_UserGuide* " [9] to modify the constraints based on the actual situation of the board to adapt to actual usage needs.

IP clock solution

10G MAC+PCS IP The clock used by the data link has 3 Three: o_usrclk , o_pclk_tx , o_pclk_rx , the clock scheme is shown in Figure 2-19 .

- o_usrclk Enter clock and IP for user data Data output clock, clock frequency is 156.25MHz ;
- o_pclk_tx for internal PCS Tx Data transmission clock, clock frequency is 161.1328125MHz ;
- o_pclk_rx for internal PCS RX Data receiving clock, the clock frequency is 161.1328125MHz .

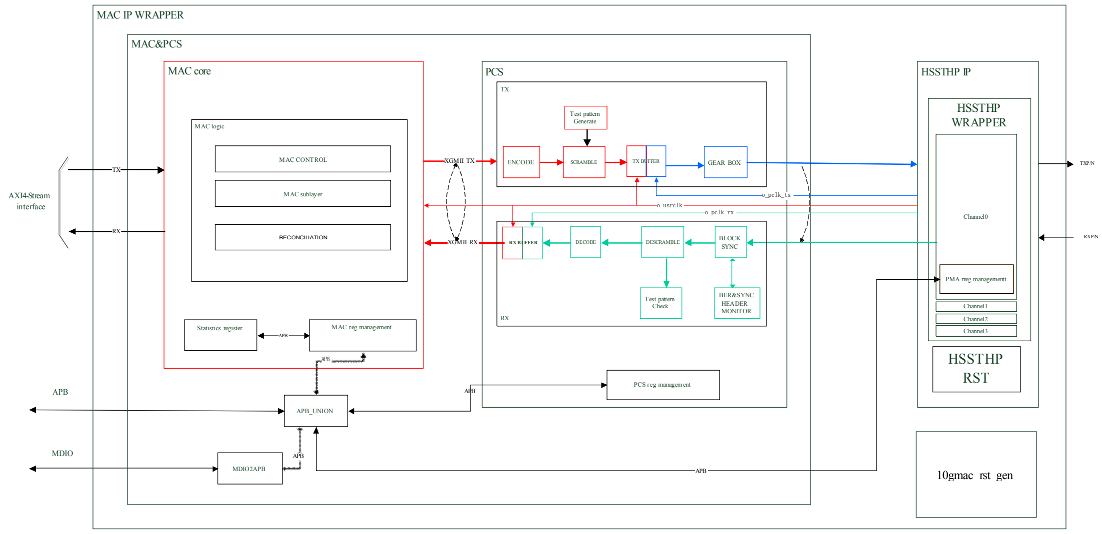


Figure 2-19 10G MAC+PCS Clock scheme block diagram

Resistance correction

the HSSTHP used .

1. scene one

IP Use HPLL And HPLL Constrained to HSSTHP_4 , at this time IP port o_p_calib_done Valid; the user needs to reset and release i_ext_rstn after o_p_calib_done is pulled high .

2. Other scenes

For other application scenarios besides the above "Scenario 1", at this time IP port o_p_calib_done Invalid, the user needs to change <project_path>/rtl/ipsxe_10gmac_hssthp/ipm2t_10gmac_hssthp_tmplc.v The contents in are manually transplanted into the project, the corresponding ports are connected, and in .fdc Add physical constraints to the file. See Table 2-46 for the port meanings of the instantiated modules in ipm2t_10gmac_hssthp_tmplc.v .

Table 2-46 Resistance correction port description

Interface name	clock domain	input Output _	describe
P_CFG_RST_HPLL	async	enter	Resistance correction module reset port, high effective; reset is only valid during resistance correction; InExample _ Design adopted in hsst_cfg_soft_rstn Corresponding reset.
P_CFG_CLK_HPLL	clock	enter	Resistance correction module clock port, connected to APB When configuring bell; in Example Design pclk is used in .
p_calib_en	P_CFG_CLK_HPLL	enter	Resistance correction module enable port, fixedly connected to 1 ;
p_calib_done	P_CFG_CLK_HPLL	output	Resistance correction module completion indication signal 1 : Indicates that resistance correction is completed; 0 : Indicates that the resistance correction has not been completed;

uart_ctrl Module read and write operation example

1. Read operation

Read address 0x000001 The data: ″ 0x000001 ″ + ″ 0x72 " , which is 0x00000172 .

2. write operation

To address 0x000001 Write 0x02 : ″ 0x00000002 ″ + ″ 0x000001 ″ + ″ 0x77 ″, for 0x0000000200000177 .

Flow control mechanism description

1. Flow control configuration

10G MAC+PCS IP Provides two flow control mechanisms: PAUSE and PFC . The enable control of the two mechanisms can be controlled through ports or registers. For details, see ″ 2.5.1 1 IP Interface List ″ and ″ 2.6.1 2 Configuration status register ″

- Uncheck ″ IEEE802.1Qbb Priority-based Flow Control ”: I P _ After instantiation, there is only PAUSE inside ;
- Check ″ IEEE802.1Qbb Priority-based Flow Cont r o l ” : I P PAUSE is included internally after instantiation

  and PFC , PAUSE Enable is turned on by default.

Notice:

Only one of the flow control mechanisms can be selected during use.

2. PON/POFF Features

10G MAC+PCS IP for PAUSE/PFC Flow control provides two functions: PON and POFF .

- PON Enable: When 10G MAC+PCS IP TX detected The falling edge of the *req [5] signal of directional flow control will send a control frame with a corresponding time parameter of 0 at the time point when the control frame can be sent.
- POFF Enable: 10G MAC+PCS IP After the set control refresh time is reached, a time point at which the control frame can be sent will be found to send a new control frame.

Take PFC For example, in PON and POFF Enable, PFC When the corresponding function is enabled, PFC The sending mechanism is shown in Figure 2-20 .

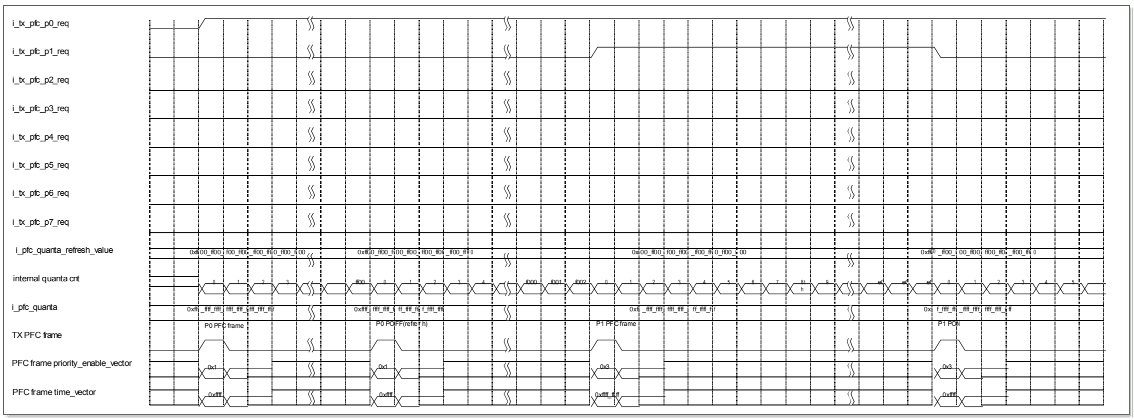


Figure 2-20 PON and POFF Enable PFC Sending mechanism diagram

IP Debugging means

Example Design MediumDebugCore _ and output status signals can monitor 10G MAC+PCS IP link status and send and receive data.

DebugCore For the signal list and status indication signal list, please refer to Table 2-8. and Table 2-5 .

Example Design UART in Can read IP The value of the status register is used to monitor the link status.

5 Such as PAUSE i_pause_req , or PFC i_tx_pfc_p0_req _ wait.

UART For the use of modules, please refer to ″ 2.4.3 1 u a rt_ c trl ”.

Chapter 3 Appendix

Reference documentation

[1] Pango_Design_Suite_Quick_Start_Tutorial

[2] Pango_Design_Suite_User_Guide

[3] IP_Compiler_User_Guide

[4] Simulation_User_Guide

[5] User_Constraint_Editor_User_Guide

[6] Physical_Constraint_Editor_User_Guide

[7] Route_Constraint_Editor_User_Guide

[8] UG050008_Titan2 Series FPGA High Speed Serial Transceiver（HSSTHP）User Guide

[9] UG051004_Titan2_HSSTHP_IP_UserGuide

Glossary

1

10GBASE-R An IEEE 802.3 physical coding sublayer for serial 10 Gb/s operation. (See IEEEStd 802.3, Clause 49.)

A

APB Advanced Peripheral Bus

C

CDR Clock Data Recovery

H

HSSTHP High Speed Serial Transceiver High Performance

L

LH Latching High

LL Latching Low

M

MDIO Management Data Input/Output

MAC Media Access Control

N

NR Non Roll-over

P

PHY Physical

PCS Physical Code Sublayer

PMA Physical Media Attachment

PAUSE MAC Control PAUSE operation

PFC MAC Control PFC operation

R

RD Read

W

WR	Write

缩略语表

D

DEVAD	device address

I

IPC	IP Compiler

P

PDS	Pango Design Suite
PCE	Physical Constraint Editor
PRTAD	port address

U

UCE	User Constraint Editor

statement

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